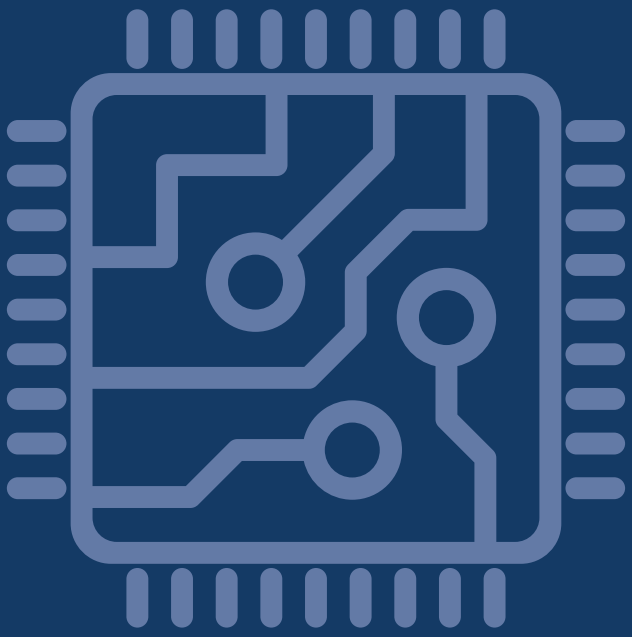
Recovery, Transformation and Resilience Plan



PERTE Chip Microelectronics & Semiconductors

TECHNICAL REPORT
May 2022

Funded by the European Union
NextGenerationEU

GOBIERNO DE ESPAÑA

#PlanDeRecuperación

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1. Relevance of the semiconductor sector

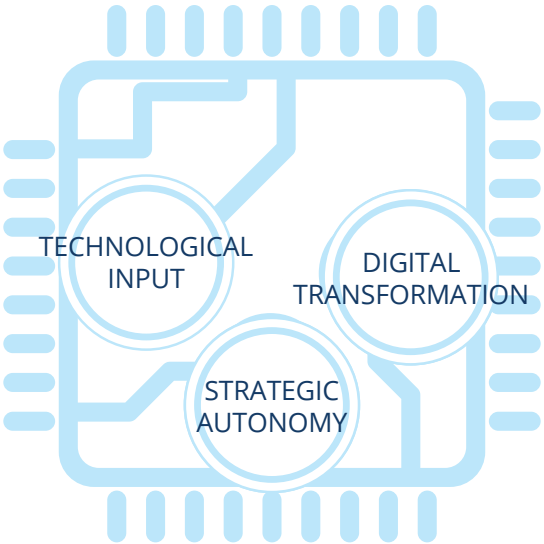
Sector characteristics

The semiconductor sector can be defined as the set of industrial activities aimed at designing and manufacturing microprocessors[1] and other electronic elements contained in the range of technological products and services that sustain our society's digital economy.

Semiconductors can be found in virtually any sector: from the smartphones, computers and tablets used on a daily basis to industrial sectors such as the production of automobiles and medical equipment and even cross-disciplinary applications like the energy and telecommunications sectors or the data centres that support the internet and its digital platforms.

Thus, the semiconductor is a basic input for all technology sectors and therefore it is of geo-strategic importance within the context of the digital transformation of the economy.

The shortage of semiconductors on a global scale prompted, among other factors, by the global supply chain disruptions caused by the pandemic has, therefore, led to factory shutdowns in a wide range of sectors, from automobiles to medical devices[2]. EIn the automotive sector, for example, production fell by one third in some Member States in 2021, which highlighted even further the dependence of one of the most important industries in the European Union on a very small number of stakeholders within a complex geopolitical setting[3].



1. Also known as chips, microchips, processors, etc. These and other similar terms will be used in this document.
2. *'Understanding the global chip shortages'*, J.P. Kleinhans & J. Hess, Stiftung Neue Verantwortung (2021).
3. Comunication *"Una ley de chips para Europa"*. COM(2022) 45 final.

However, to pinpoint the causes of this issue it is necessary to define the characteristics of the complex supply chain in this sector.

Description of the value chain

The semiconductor sector can be described as a capital- and R&D-intensive global sector with important entry barriers due to the investment volume and the sophistication of its technology, featuring inelastic supply and oligopolistic structures that strain global supply chains in sectors such as automobiles, telecommunications or consumer electronics.

The semiconductor manufacturing process can be separated into the design and the manufacturing stages. Based on this initial structure, certain distinct roles can be discerned within a global, highly inter-dependent, value chain with strong geographical concentration.

Design

The architecture, electronic components and their arrangement are determined in the design. This is the most R&D-intensive stage, with the greatest added value, in which the intellectual property (IP) is defined. Software design companies (EDA tools) are also involved at this stage. These companies exercise control over the intellectual property rights of their patents and licences, which are used by the manufacturers.

The business models found at this stage include companies exclusively devoted to "pure" design, as well as companies present at other stages of the value chain such as commercialisation (this would be the case of a "fabless" company) or even integrating the entire value chain (referred to as an "Integrated Device Manufacturer" or IDM). These models are outlined in the following paragraphs.

Fabrication

Fabrication takes place in foundries. Fabrication comprises the chip manufacturing stage, starting from silicon wafers and following a series of complex, highly automated, sequential processes[4]. This stage is known as the front-end process.

The foundries, most of which are located in Asia, represent a bottleneck in the value chain. They are influenced by numerous factors, including trade sanctions, demand disruptions (during the pandemic) or even lack of availability of natural or energy resources (drought, power outages, fires, etc.).

One of the ways to measure the technological level of a semiconductor is through node size. The smaller the node size, the denser the transistors are and, thus, the greater the performance in a smaller size.

4. Oxidation and coating, photolithography, chemical etching, doping, metal deposition, etc. These phases may be repeated several times to form successive layers.

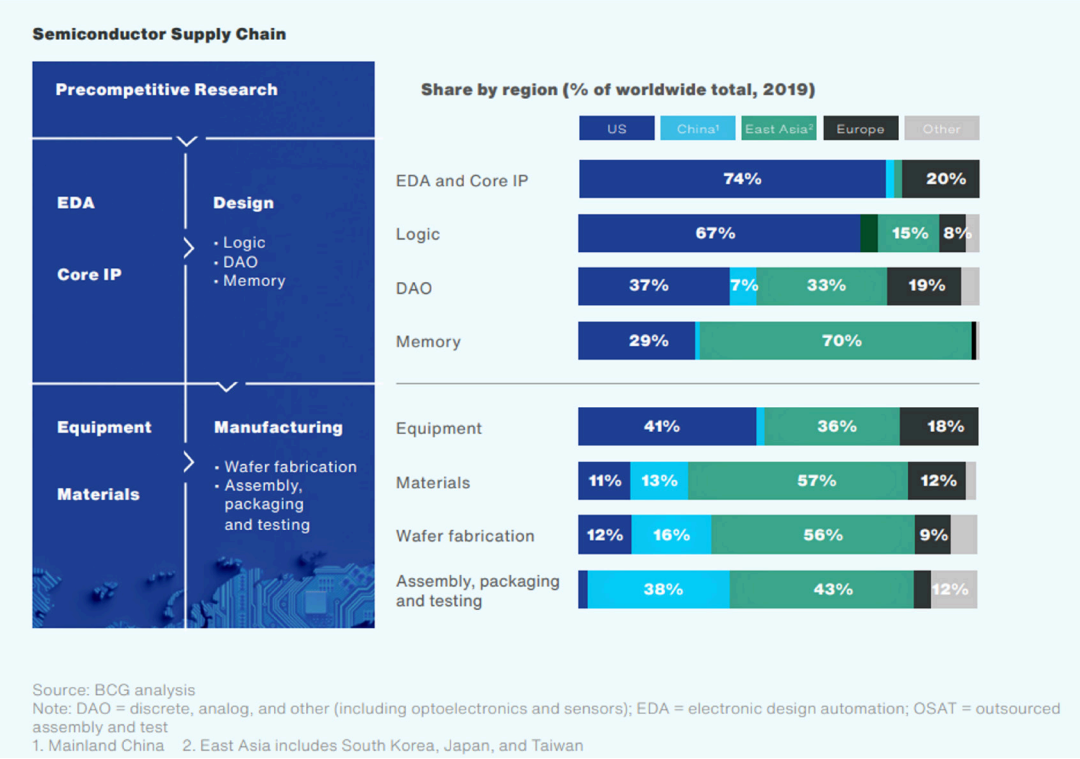
Foundries can now manufacture sizes as small as 5 nm, but they are progressing towards the next generation of microchips, beyond 5 nm, and to this end they require significant investment volumes[5].

Participants in the fabrication stage include suppliers of key resources like the manufacturing equipment and materials (silicon wafers, chemicals, industrial gases, etc.). In this field, there are specific niches and segments that play essential roles in the fabrication stages.

The final stage of the fabrication process, known as the back-end process, consists of packaging, assembly and testing. At this stage, the wafers are cut into dice, the connections are created between the printed circuits and the wafers are coated with a protective layer to protect them from external agents. Testing also takes place at this stage to ensure that each chip functions correctly.

The back-end phase tends to become vertically disintegrated from the fabrication, strictly speaking, of silicon wafers, and there a number of specialised companies devoted exclusively to these activities.

The following graph shows the degree of geographical concentration of the value chain:



"Strengthening the semiconductor supply chain in an uncertain era", Boston Consulting and SIA (Semiconductor Industry Association)

5. To give an idea of the order of magnitude, the 3-nm chip plant that Samsung has announced it will build in Texas will cost USD 17 billion. https://www.electronicdesign.com/technologies/embedded-revolution/article/21182155/electronic-design-samsung-plans-to-build-17-billion-chip-plant-in-texas-by-2024

Generally speaking, the United States is the leader in the design phase, except in the memory chip segment, where Asia takes the lead.

The manufacturing phase takes place primarily in Asia, with a high concentration of foundries in Taiwan and South Korea, generating a bottleneck that strains manufacturing of cutting-edge chips, those smaller than 10 nm, which are used in computers, telecommunications, data centres and consumer electronics.

In Europe there is some local production capacity for mid-range performance chips (greater than 22 nm) to cover the needs of part of the automotive and industrial instrumentation industries..

Business models

To conclude this approach to the sector, it is necessary to introduce two common business models:

IDM (Integrated Device Manufacturer)

IDMs integrate the design and manufacturing phases, and their greatest representatives are Intel and Samsung. By integrating the design and manufacturing phases, IDMs benefit from greater coordination between their teams and do not need to subcontract production, which leads to lower costs and less dependence on third parties. In addition, they are more flexible because they can act as foundries for third parties or subcontract their manufacturing to other foundries during production peaks.

However, IDMs must allocate significant resources to R&D in an effort to keep their plants up to date and must also support a complex organisational system that may span everything from raw materials procurement to commercialisation.

Therefore, the IDM model currently shows a vertical disintegration trend, thus leading to specialisation in its two phases: on the one hand, fabless companies perform the design and commercialisation processes, but they subcontract specialised fabrication to foundries.

Fabless

Fabless chip manufacturers are involved in the design and commercialisation phases, but may also participate in the testing and packaging phases, lwhich distinguishes them from designers exclusively focused on the development of Intellectual Property (IP).

By dispensing with fabrication and logistics complications, they can focus on innovating microchip designs and can also cover wider fabrication ranges by outsourcing to different foundries. This lighter-weight structure even makes it possible for small enterprises and start-ups to compete in the market.

On the other hand, they are totally dependent on external foundries, their workloads and the exclusivity agreements they may have in place with other clients.

Starting in the 90s, the first companies incorporated directly as fabless began to appear.

European context

Despite modest market shares in the global value chain, Europe has significant strengths in specific areas of the value chain.

Firstly, in the academic and scientific field, Europe is well-positioned worldwide, with benchmark institutions such as the IMEC (Belgium), the CEA/LETI (France) and Fraunhofer (Germany) [6].

In the design field, there are leading companies specialised in chips for industrial electronics or the automotive industry. There is also a growing ecosystem of research centres and small companies specialising in processors and advanced accelerators for use in high performance computing and Artificial Intelligence.

The continent is also well-positioned globally in certain key supplies such as machinery, chemicals and raw materials like substrates and gases. One of the most significant cases is that of the Dutch company ASML, the only global supplier of high-precision photolithography equipment for manufacturing the most advanced chips under 7 nm.

Even so, Europe only manufactures a share of about 10% of the total volume worldwide. Moreover, it only produces mature technology nodes (the foundries only work above 22 nm), used in the automotive industry, industrial automation and the aerospace industry, sectors that are traditional drivers of European industry.

Therefore, there is a dependency on the manufacturing capacity and on the companies that design the latest chips (in the vicinity of 5 nm) used in cutting edge sectors such as telecommunications, consumer electronics and data centres.

This decreasing trend is partly explained by the progressive relocation process seen in the consumer electronics, mobile telephone and telecommunications sectors in recent decades, in which investments could not keep pace when confronted with the absence of technology sectors to support the industry.

While the EU has a consolidated policy in place to reverse this trend with a view to increasing the Union's digital sovereignty and strategic autonomy, the turning point came with the **Communication about the Digital Decade**[7],nnwhich established **the quantitative goal of reaching at least 20% of world production of cutting-edge semiconductors (below 5 nm and aiming at 2 nm) by 2030.** This entails increasing current production volumes fourfold, bearing in mind that global production will double in order to meet the demands of the digital transformation.

This objective was transferred to the Decision establishing the 2030 policy programme

6. https://ec.europa.eu/commission/commissioners/2019-2024/breton/blog/how-european-chips-act-will-put-europe-back-tech-race_en
7. https://eur-lex.europa.eu/legal-content/ES/TXT/HTML/?uri=CELEX:52021DC0118&from=en

"Path to the Digital Decade", the main instrument for planning, governance and monitoring of the EU's digital policies, which will make it possible to conduct a coordinated assessment of the goal of producing 20% of the semiconductors by 2030[8].

However, the true challenge here is not in terms of volume but rather the capability to produce cutting edge semiconductors. In response to this shortcoming, the EU is rolling out a series of instruments designed to mobilise investments, including, in particular, a European policy specifically designed for electronics and semiconductors: the recent proposal of the **European Chips Act,** announced on 8 February 2022, to confront the semiconductor shortage and strengthen Europe's technological leadership[9].

The European Chips Act establishes a framework for bolstering investment in order to help it meet the goal of 20% of world production by 2030. It is broken down into three pillars:

- **Pillar I. Creating the Chips for Europe Initiative** with the aim of supporting the development of large-scale capacities by investing in infrastructures for research, development and innovation in order to strengthen advanced design capacities, system integration and EU chip production.
- **Pillar II. Creating a framework for ensuring security of supply** by attracting investments and enhanced production capacities in semiconductor manufacturing, as well as in advanced packaging, testing and assembly through integrated production facilities and foundries.
- **Pillar III. Establishing a coordination mechanism between the Member States and the Commission** to strengthen the collaboration with and between the Member States, monitor the supply of semiconductors, estimate demand and anticipate crisis situations and shortages.

Although the European Chips Act will represent the key element of the EU's semiconductor policy, there are a number of other EU programmes for stimulating the microelectronics industry, such as:

- **European High Performance Computing Joint Undertaking (EuroHPC JU)**[10]. An alliance between the Commission and the 27 Member States (plus a few associated countries) to promote supercomputing in Europe with the specific objective of acquiring, building and deploying in Europe a network of benchmark supercomputers worldwide.
- **European Processor Initiative (EPI)**[11]. A European consortium founded in 2018 to design processors and high-performance accelerators. Composed of 28 partners from 10 countries, led by the French firm Bull SAS and with Spanish

8. https://digital-strategy.ec.europa.eu/en/library/proposal-decision-establishing-2030-policy-programme-path-digital-decade
9. https://ec.europa.eu/commission/presscorner/detail/es/ip_22_729
10. https://eurohpc-ju.europa.eu/
11. https://www.european-processor-initiative.eu/project/consortium/

participation by BSC-CNS (a leader in the RISC-V-based accelerator component) and Semidynamics. The EPI's projects are aimed at developing general-purpose HPC microprocessors, accelerators, architecture and use cases for the automotive industry. A new funding agreement (Specific Grant Agreement 2[12]) was recently issued, which seeks to continue its predecessor's lines of work.

- **Key Digital Technologies Joint Undertaking (KDT JU).** This is the main European company stimulating Innovation related to semiconductors. The JU is funded by the industry, the Commission and the Member States. It arose from the Electronic Components and Systems for European Leadership (ECSEL) initiative, which, during its 7 years of execution, financed 92 projects with a total budget of € 4,800 million[13]. For the 2021-2027 period, it was renamed as KDT JU, increasing the project's ambitions (€ 7,200 million) and its topics, placing greater emphasis on photonics and software.

  The European Chips Act will rename the KDT JU as Chips JU, granting it broader competence and more ambitious objectives and increasing its budget to € 11,000 million to strengthen existing research, development and innovation, ensure the use of advanced semiconductor tools, pilot lines for prototyping, testing and experimenting with new devices for innovative real-life applications, providing training and promoting a thorough understanding of the semiconductor ecosystem and value chain.

- **The European Alliance on Processors and Semiconductor Technologies**[14]. In July 2021 the Alliance on Processors and Semiconductor Technologies was established as a benchmark industrial forum to identify gaps in the semiconductor value chain and promote its development, focusing especially on semiconductor design and manufacturing activities. The Alliance provides strategic advising on the semiconductor policy in the EU.

- **The IPCEI on Microelectronics and Communication Technologies (IPCEI ME-CT)**[15]. EThe IPCEI ME-CT is one of the main instruments for promoting semiconductors in the EU. It aims to strengthen semiconductor production in Europe, encompassing the entire microchip value chain, from design to fabrication and packaging, thus reducing the dependence on third-party countries, ensuring the long-term sustainability of the sector and covering the European market's critical needs. The IPCEI ME-CT has been pre-notified to the Commission with 11 Spanish candidates. The Commission is currently in the assessment phase, awaiting a final approval decision.

12. https://www.bsc.es/es/research-and-development/projects/epi-sga2-sga2-specific-grant-agreement-2-the-european-processor
13. https://www.kdt-ju.europa.eu/
14. https://digital-strategy.ec.europa.eu/en/policies/alliance-processors-and-semiconductor-technologies
15. The Important Projects of Common European Interest are state aid instruments that require the participation of several Member States to achieve transformational, cross-border and high impact effects on industrial value chains.

- **Microelectronics IPCEI (prior IPCEI)**[16]. In addition, it is worth mentioning the existence of a previous IPCEI on microelectronics, approved in December 2018. The aim of this first IPCEI was to enable the research and development of innovative components and technologies (chips, integrated circuits and sensors, for example) that can be integrated into a large set of subsequent applications. The countries that participated in the first IPCEI were France, Germany, Italy, Austria and United Kingdom.

16. https://www.ipcei-me.eu/what-is/

2. Strategic assets for the deployment of the PERTE

After analysing the global scenario of the complex semiconductor sector value chain and the specific situation of the European industry, it is necessary to deploy an instrument for promoting the Spanish semiconductor ecosystem that will take a decisive step towards the transformation required by the sector.

It is in this context that the Government of Spain has launched this Strategic Project for Economic Recovery and Transformation of Microelectronics and semiconductors (PERTE Chip, Spanish acronym), with a budget of EUR 12.25 billion, aimed at bolstering the Spanish microelectronics and semiconductor industry value chain from an integrated perspective, spanning all the phases involved in the conception, design and fabrication of chips.

The PERTE arises from the need to increase microchip production capacity in the European Union and it is logically aligned with other EU policies, particularly the European Chips Act, as the sector in Spain has characteristics that are similar to those of the other Member States.

However, within the diverse fields of action of the European Chips Act, this PERTE focuses on fostering those strategic assets in which Spain is best positioned overall with a view to having a stronger stimulus effect on the sector, but also deploying cross-disciplinary measures that keep the focus on innovation across the value chain as a whole.

Thus, a series of strategic assets are described that hold a key position within the diverse microelectronics and semiconductor sector in Spain.

RISC-V

Firstly, it is important to note the significance of processors with reduced instruction sets, especially RISC-V, which has led to a change of paradigm compared to traditional architecture. This open standard instruction set architecture, which defines processors and accelerators, enables the design of devices for a compatible software ecosystem. RISC-V is becoming a global phenomenon that is freeing the ecosystem of patented hardware designed outside of Europe[17]. RISC-V opens the door for Europe and the world to design and construct native processors' technology aimed at a common software ecosystem.

Proof of the success of this architecture is the interest aroused by the leading start-ups in the sector among companies that own traditional types of architecture.

17. The term x86 architecture refers to instruction set architecture (ISA) developed by Intel or AMD, named for its first predecessor, Intel 8086, developed in the late 70s. This type of architecture is commonly used in PCs and offers high performance, unlike RISC architectures, which are lighter and consume less energy because they are designed for the smartphone market, in which the leading company is ARM. Both of the ISA models prevailing on the market are distributed under licence.

The high-level geopolitical approaches being taken in the EU would not be possible without the revolution being caused by RISC-V. In fact, RISC-V holds a preeminent position in *Pillar I Chips for Europe* of the European Chips Act.

In this regard, the Barcelona Supercomputing Center – Centro Nacional de Supercomputación (BSC), supercomputing leader in Spain and an international benchmark in this field, is a key figure. It is also a global leader in the development of RISC-V and one of the first institutions to promote this architecture in the EU, as was also the case decades ago with the early steps of ARM architecture[18]. The BSC is one of the central assets of the computing sector in this country, with a team of more than 800 people[19].

Integrated photonics

Integrated photonics[20] is a growing sector with relatively new, high added value, technology in which Europe holds a strong global position, ranking second following North America, with a 21% share[21].

One of the competitive advantages of photonics is its capacity to be integrated in combination with electronic chips, thus increasing their performance and versatility. In fact, this feature is what makes photonics a strong cross-disciplinary technology that is used not only for connecting telecommunications cables and data centres, but is also gradually extending to cutting edge sectors such as healthcare, computing and 5G, because its ability to integrate elements such as sensors or actuators used for IoT or automated driving applications.

Therefore, integrated photonics is shaping up to become a technology area that could, in the medium to long term, act as a bridge between current technologies and the quantic technologies of the future.

Spain has a complete, well-established value chain that encompasses all the links of the value chain: ranging from R&D&i centres to design, fabrication, packaging, assembly and testing equipment. There is also a variety of end consumer business profiles for the different photonic elements and devices.

Spain is very well positioned worldwide with the ITEAM[22] photonics group at the Polytechnic University of Valencia, University of Vigo and other benchmark centres, as well as a significant number of spin-offs created in relation to the university system.

18. Europe had a European champion, the British company ARM, which is the main supplier of low consumption processors for smartphones and low consumption electronics in general, in the field of IoT and laptops. ARM was bought by the Japanese company Softbank in 2016, thus losing its European status. Subsequently, the US company NVIDIA attempted to acquire it but the purchase agreement was discarded in February 2022, partly due to difficulties related to competition regulations. ARM supplies IP but has no fabrication capacity.
19. https://bsc.es/
20. Integrated photonics comprises all the activities that use photonic technology and applications geared towards the design and fabrication of microchips.
21. Mordor Intelligence. 2017 data.
22. Telecommunications and multimedia applications Institute.

En el marco europeo, la fotónica integrada cuenta con un papel reservado dentro de las actividades de la Iniciativa Chips para Europa de la Ley Europea de Chips.

Quantum chips

Quantum computing is the branch of IT that uses the principles of quantum mechanics to enable a multitude of operations to be performed simultaneously, thus increasing processing performance and information security and overcoming the barriers of classic computing. The smallest unit of information is called a qubit (in contrast with the bit in classic computing) and the quantum computers that use them can generate these qubits in different ways and with different technologies.

The world's quantum computing centres are currently located in the United States and Europe, where initiatives like Quantum Flagship [23] exist for progressing in the development of quantum simulation and applications.

In relation to the European initiatives, the Government of Spain approved the Quantum Spain plan in December 2021 with the aim of promoting quantum computing in Spain and strengthening the Spanish computing system through a series of activities based on the following concepts:

- Quantum algorithm
- Creation of a quantum computer in production based on superconductor currents
- Equipping classic computers for simulation
- Talent

One essential part of this plan consists in the construction of quantum chips with gradually increasing capacities, operating on up to 20 qubits and also offering cloud access to the entire Spanish educational system and business sector.

Spain has a healthy number of research groups on quantum computing technologies, such as the ICFO, CSIC, BSC and UPM[24], which are forerunners in the creation of open space and fibre quantum communication devices and their integration in commercial networks, and the IFAE[25], which leads European projects for the creation of quantum optimisers.

Clean Rooms of micro and nanofabrication (Micronanofab)

Spain also has a Singular Scientific and Technical Infrastructure (ICTS) specific to microelectronics constituted by the Network of Micro and Nanofabrication Clean

23. https://qt.eu/
24. Photonic sciences Institute, Spanish National Research Council, Barcelona Supercomputing Center, Polytechnic University of Madrid
25. Institute for High Energy Physics

Rooms (MICRONANOFABS). EThe main node of MICRONANOFABS is the Institute of Microelectronics of Barcelona-National Microelectronics Center (IMB-CNM, CSIC), which through its Clean Room, which has its own staff that develops different R&D projects, in addition to making available to the scientific or business community its prototyping and manufacturing capacity of small series oriented to electronic devices and systems, mainly in the "More than Moore" field.

The Clean Room has different fields of work, such as integrated photonics, wide-bandgap semiconductors (for power applications and harsh environments), micro and nanoelectrodes (for chemical sensors), graphene technology (biomedicine) or silicon micromachining (for MEMS applications).

In this way, it has contributed to the development of several international projects, incorporating its own technology for CERN, as well as different satellite constellations and space missions.

The Clean Room also offers training and hands-on training in the field of micro and nanoelectronics.[26]

The driving sectors

Having identified the sector's strengths from a supply perspective, the strategic sectors that drive semiconductor demand are outlined, as natural consumers of these types of components.

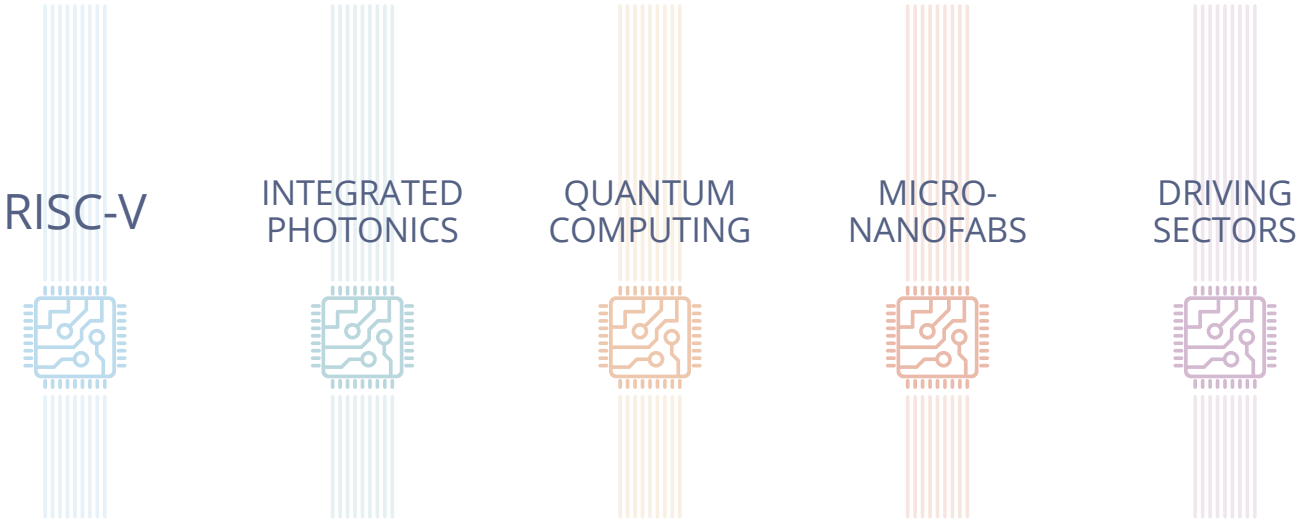
Firstly, the automotive sector should be mentioned, in which Spain ranks second in Europe in vehicle manufacturing, first in the industrial vehicle category, and eighth on the global market. The vehicle manufacturing industry is supported by a significant, competitive industry of automotive component suppliers that ranks fourth in Europe. The automotive component sector generates 75% of the added value of the vehicle[27]. It is no coincidence that, in such a dynamic, automated sub-sector strong on exports and present throughout the country, Spain boasts cutting edge companies in the design of electronic sub-systems for automotive use, and that they even hold leading positions worldwide in certain segments, as noted by the European Commission[28].

It should also be noted that the progress made in self-driving and electric vehicles will boost the need for sensors and 5G connectivity, rendering vehicle electronics an increasingly significant part of the added value of a vehicle.

26. Some of the successes of the Clean Room include radiation sensors deployed at CERN, devices for space applications deployed on the OneWeb satellite constellation and the Solar Orbiter, Bepi-Colombo and future Juice space missions, as well as pH measurement devices including medical products sold in pharmacies.
27. https://www.sernauto.es/blog/sector-componentes-de-automocion-en-2021/
28. Vice-President Vestager.*"Spain is a European global champion when it comes to the design, development and manufacturing of electronic components for cars' passive keyless entry, with more than 60% of the global market share".* https://ec.europa.eu/commission/presscorner/detail/en/SPEECH_22_888

In terms of industrial process automation, Spain is the third producer and exporter of machine tools in the European Union and ninth in the world[29]. With exports accounting for 80% on average, this sector exports products around the world, featuring a strong focus on R&D and high consumption of electronic devices to meet the automation needs of its main markets; the automotive industry, capital goods and the aeronautical and aerospace industry.

Moreover, there is a significant carry-over effect from other technology sectors such as telecommunications, the aerospace industry, defence material, rail transport and infrastructure construction.



29. https://www.afm.es/es/quienes-somos/sector-maquina-herramienta

3. Definition and structure

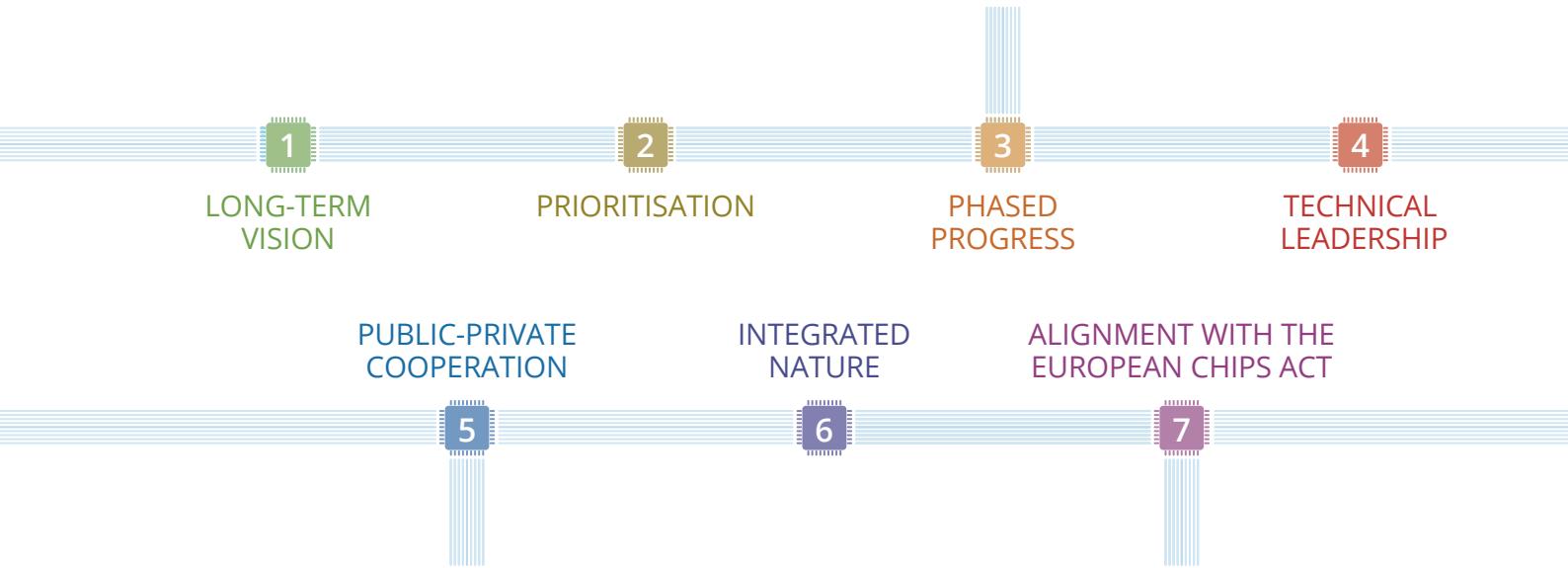
In light of the above, **PERTE Chip is defined as a strategic initiative that aims to develop the design and production capacities of the microelectronics and semiconductor industry in this country so as to generate an important ripple effect not only in technology sectors but in the Spanish economy as a whole.**

The fertile ground for investing in innovative technology afforded by the European Chips Act poses a unique opportunity within a changing geopolitical situation in which traditional offshore production models do not always offer a comparative advantage over the strategic sovereignty principles of the Union.

The project approach is based on 7 principles that are present throughout all of its activities:

1. **Long-term vision.** This PERTE sets out a series of actions to be taken in a technically complex, global sector with an extended timeline for execution. Both the public support and the private initiatives must be conceived as long-term elements designed to continue focusing on innovation throughout the entire value chain.
2. **Prioritisation.** In such a capital- and knowledge-intensive sector as this one, highly significant investments are required to ensure a sufficient impact on a highly competitive global value chain. Attempting to cover too many topics would jeopardise the success of the actions.
3. **Phased progress.** Because of the elevated technological risk and the investment volume, it is essential to implement a timeline that will ensure accurate, coordinated progress throughout each of the phases, both technical and financial.

4. **Technical leadership.** The semiconductor sector is one of the most technologically complex industries around. Therefore, the PERTE must be led from a technical perspective that prevails over decisions of any other nature.
5. **Public-private cooperation.** The PERTE will deploy the cooperation mechanisms needed to promote public and private investing geared toward shared goals, ensuring coordinated actions by the public authorities, the industry, universities and research centres.
6. **Integrated nature.** The project is designed as an integrated initiative that spans the entire value chain of the semiconductor industry and complements other PERTES passed by the Government, particularly those with a strong technological and cross-disciplinary focus[30].
7. **Alignment with the European Chips Act.** The PERTE is aligned with the European Chips Act, directly contributing to its objectives and generating synergies while also complementing other initiatives developed by other Member States and other EU institutions.



Thus, taking inspiration from the aforementioned principles, with a view to achieving its main objective, the PERTE Chip will be arranged into a number of specific actions distributed across four components that encompass the different fields of the value chain.

— **COMPONENT ONE - BOLSTERING SCIENTIFIC CAPACITY.** With a long-term vision, this component is aimed at bolstering R&D&i capacities, focusing on cutting-edge microprocessors or with alternative architectures, integrated photonics and quantum chips and continuing the works of the IPCEI ME-TC.

30. Such as the PERTE for Renewable Energy, Renewable Hydrogen and Storage (PERTE ERHA), the PERTE for the Development of Connected, Electric Vehicles (PERTE VEC) and the PERTE for Digitalisation of the Water Cycle.

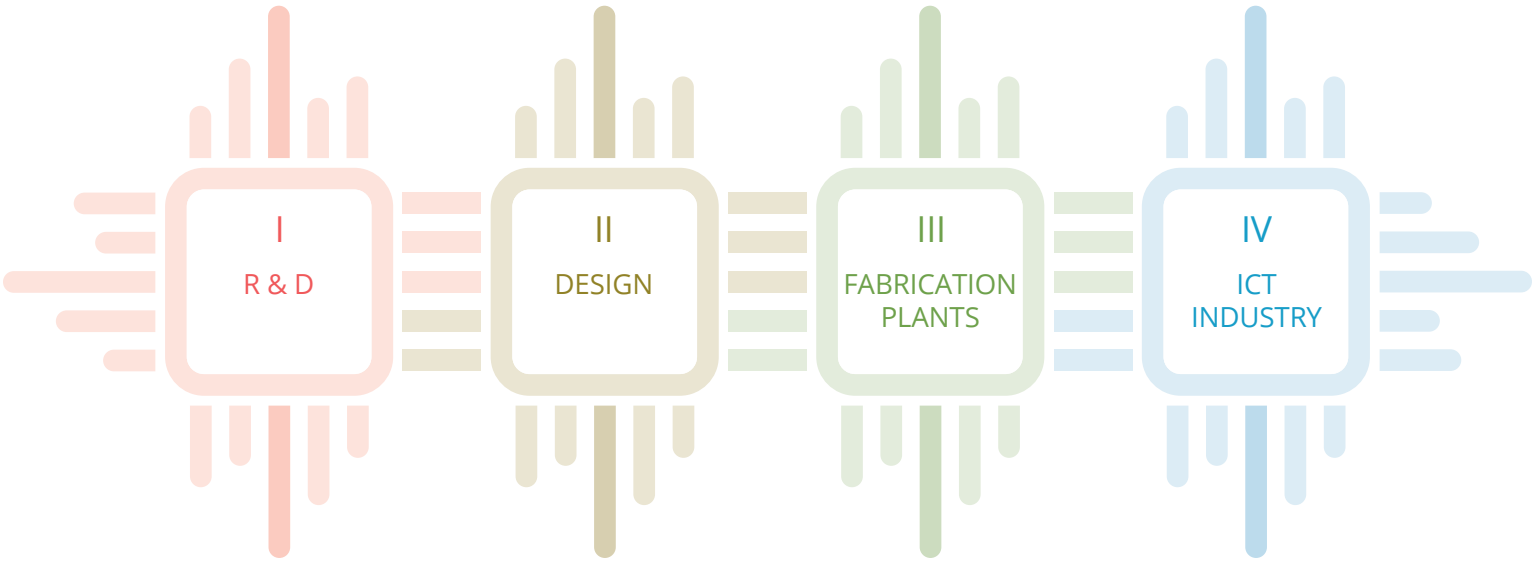
— **COMPONENT TWO - DESIGN STRATEGY.** The second component, with its sights on the medium term, aims to strengthen the Spanish design ecosystem by creating fabless companies for the design of cutting-edge microchips or with alternative architectures, by developing test pilots and creating a network for education, training and skills-building to strengthen the sector's human resources.

— **COMPONENT THREE - CONSTRUCTION OF FABRICATION PLANTS IN SPAIN.** This component focuses on increasing industrial production capacities by building foundries with cutting edge technology (nodes of 5 nm or less) and mid-size technology foundries (above 5 nm), possibly as part of the European Chips Act.

— **COMPONENT FOUR - STIMULATING THE ICT MANUFACTURING INDUSTRY IN SPAIN.** The objective of this component is to conduct a detailed assessment of the situation in the semiconductor industry in order to deploy incentives for the creation of an ICT product manufacturing industry that will act as a driving force, or by launching public aid schemes for the semiconductor entrepreneurship ecosystem.

As these actions require a strong element of innovation, a certain degree of flexibility will be applied in developing them so as to orient the actions as the project progresses, within reasonable margins of technological uncertainty.

To ensure the coordination, effectiveness and consistency of the measures, a governance system is created, to be headed by the special commissioner for semiconductors.



3.1. COMPONENT ONE BOLSTERING SCIENTIFIC CAPACITY

Reference framework

The objective of this component is to bolster the R&D&i related to semiconductors in order to prolong the public support for the Spanish Science, Technology and Innovation System in strategic areas that will make it possible to define the characteristics of the next generation of microprocessors.

There are currently public support schemes for R&D&i in the semiconductor sector in place at the national and EU levels. This is the case of the EuroHPC JU, the EPI, the KDT JU (future Chips JU), and the diverse actions funded under the Horizon Europe and Digital Europe programmes.

However, it is necessary to focus our efforts on those technologies with the strongest potential for Spain. In this regard, the IPCEI on Microelectronics and Communication Technologies, through its two Expressions of Interest, has helped identify cutting edge technology areas in which Spain is well-positioned, such as the design of alternative architectures like RISC-V and the field of integrated photonics. An initial budget allocation exists for these areas, pending final approval by the European Commission. However, to maintain the spill over effects of this European project, it is required to allocate additional resources.

The actions deriving from this component must necessarily be aligned with the Chips Joint Undertaking programmes and Pillar I of the European Chips Act. Therefore, efforts shall be made to ensure that they also contribute to the different European programmes.

In the field of quantum computing, steps should be taken to create a sense of continuity with the Quantum Spain initiative, taking these actions to the next level.

To this end, firstly, it is necessary to solve quantum computing optimisation issues in order to respond to scientific problems that are inaccessible through classic computing and, secondly, this must be accompanied by the required innovative software and hardware development.

Actions

Action 1. Development of R&D&i on cutting-edge and alternative architecture microprocessors

The goal of this action is to promote R&D&i around the design of alternative architectures such as RISC-V with a view to progressing toward future generations of chips.

The scope of the action should include, among other items, accelerators that increase computing performance but also general purpose processors, to make them lower

on energy consumption and more highly integrated, thus achieving a greater use of cross-disciplinary applications as in the automotive segment, IoT and portable devices.

The action will have an estimated budget of EUR 475 million for the 2022-2027 period.

The chosen funding instrument will identify the lines of work with the greatest potential, based on the achievements of the IPCEI on Microelectronics and relying on the capabilities of the Spanish research groups in this area..

Action 2. Development of R&D&i on integrated photonics

The objective of this action is to stimulate research, development and innovation in the area of integrated photonics, relying on leading businesses, research centres and universities in this field.

The field of application of the actions must encompass those scientific areas of the field of photonics that are directly related to the semiconductor industry and the fabrication of microprocessors, with applications in specific or cross-disciplinary sectors like telecommunications.

It is necessary to distinguish the R&D&i areas aimed at designing the next generation of photonic chips from the budding design or fabrication capacities already existing in Spain and Europe, which could fall under other components of the PERTE.

The action will have an estimated budget of EUR 150 million for the 2022-2027 period.

The chosen funding instrument will identify the lines of work with the greatest potential, based on the achievements of the IPCEI on Microelectronics and relying on the capabilities of the Spanish research groups in this area.

Action 3. Development of R&D&i on quantum chip development

The objective of this action is to stimulate research, development and innovation in the area of quantum chips, in order to progress toward the next generation of quantum chips in partnership with the leading businesses, research centres and universities in this field.

The field of application of this measure shall include any innovative activities aimed at:

- The development of annealers or quantum optimisers and programmable quantum simulators.
- The development of quantum computing software and hardware to optimise the technologies used on quantum simulation and computing platforms, so as to obtain more scalable circuits with longer coherence times and high-density qubits.

The action will have an estimated budget of EUR 40 million for the 2022-2027 period.

The chosen funding instrument will identify the lines of work with the greatest potential and strongest alignment with the interests of the PERTE.

Action 4. Budget line for the IPCEI on Microelectronics and Communication Technologies

The aim of this measure is to set a budget line for the IPCEI on microelectronics and Communication Technologies to ensure a sustained impact over the national microelectronic and semiconductors industry and maintain the positive spill over effects on the rest of participating Member States.

By this, the PERTE Chip will count with a budget line already foreseen in Components C12.I2 and C15.I5 of the Spanish Recovery Plan and there will be an additional budget line to finance innovative actives of Spanish participants.

The suitable instrument will stablish the financing terms for the pre-notified participants, subject to final Commission Decision. In this regard, in view of the variation that may arise during the notification progress, additional activities and projects in line with the objectives of PERTE Chip may be eligible for funding under this action, setting the appropriate participation mechanisms.

The action will have a budget of EUR 275 million coming from already allocated lines C12.I2 and C15.I5, plus a EUR 225 million extra line, totalling a EUR 500 million budget for the 2022-2027 period.

3.2. COMPONENT TWO DESIGN STRATEGY

Reference framework

Spain has a significant R&D&i network and superb scientific capacity for semiconductor design, in which technology areas such as integrated photonics and RISC-V architecture design, for example, stand out in particular.

However, Spanish design companies on the whole do not yet have sufficient critical mass to be competitive on a national or European level, and are often limited by a lack of knowledge or human resources, or by the inability to test their designs in advanced fabrication environments.

Therefore, it is necessary to strengthen Spain's industrial capacity in terms of microprocessor design by bolstering scientific capacity, competence and collaboration with Spanish companies and research centres in order to generate a favourable environment for the development of innovative initiatives.

It is also necessary to channel this stimulus toward more cross-disciplinary sectors, with greater immediate market viability, and this is only possible through the existence of fabless companies with sufficient critical mass to act as a driving force on the design ecosystem as a whole.

At the same time, with a view to shortening the intervals between each microprocessor generation, it is essential to have a pilot project infrastructure in place that meets the needs of the market and the research groups.

Finally, given the technical complexity and magnitude of the sector, it is important to approach it from a global perspective, seeking collaboration with European partners and aligning with the different programmes in the European Union, particularly the Chips for Europe initiative of the European Chips Act.

Actions

Action 5. Creation of cutting-edge and alternative architecture microprocessor fabless companies

The objective of this action is to establish fabless companies on a scale that enables them to design marketable cutting-edge microprocessors and processors that use alternative architectures such as RISC-V.

The initiative should not focus solely on nurturing European HPC capabilities to meet the demands of Artificial Intelligence or Machine Learning, but rather, it can and should extend its reach to other more cross-disciplinary sectors of the industry like IoT, the automotive industry (5G) or edge computing, to name a few.

In the first phase, a feasibility study will be conducted to determine the possibility of developing the project, , analysing the following aspects, among others:

- Identification of scientific and business stakeholders that meet the criteria of necessary critical mass, experience and resources to implement the initiative.
- Type of microchips that could be designed (accelerator, general purpose processor, node size, one or more fabrication ranges, etc.).
- Required number of professionals and their profiles.
- Identifying companies and sectors that could use the designs.
- Determining whether it would be feasible to add one or more of the fabrication phases in addition to the fabless (design and commercialisation) phase.
- Risk assessment, identifying technical, financial or labour limitations, among other possible constraints.
- Alignment with the framework of the EU European Chips Act.

In the second phase, building on the results of the feasibility study, the interest of possible stakeholders will be sought, and they will be asked to submit a highly detailed technical and financial business plan aimed at market feasibility in the medium term.

After analysing the proposals that best meet the interests of the PERTE, the most appropriate funding instrument shall be chosen that is compatible with state aid regulations in the European Union.

As an example, given the long construction timelines for foundries, the most mature designs should be able to come onto the market by 2025, so that they can be tested during the production plant commissioning and start-up phases, which could take place during the 2026-2027 period.

The action will have an estimated budget of EUR 950 million for the 2022-2027 period.

Action 6. Creation of pilot lines

The aim of this action is to construct semiconductor test pilot lines in Spain so that the scientific community and design companies, as well as manufacturers, can validate their prototypes across all the phases of the microprocessor fabrication value chain, from experimentation to testing, machinery optimisation, packaging and assembly, to name a few.

This will help speed up as much as possible the intervals between the different semiconductor R&D&i, design and fabrication phases by affording prompt feedback.

The pilot lines may be new or may entail enhancements on existing ones, and they should be intended for open use by the scientific, design and fabrication community, encouraging access for SMEs.

Furthermore, they must focus on the newest fabrication technologies, in line with the work programmes of European initiatives like the KDT JU or the future European Chips Act (particularly Pillar I thereof).

The action will have an estimated budget of EUR 300 million for the 2022-2027 period.

The chosen funding instrument will identify those initiatives with the greatest potential in Spain that are most closely aligned with the interests of the PERTE. In particular, an analysis will be made of the pilot lines most in demand by the design companies and scientific teams, so they can start testing their designs as quickly as possible.

Action 7. Creation of a network for education, training and skills-building in relation to semiconductors

The aim of this measure is to create human resources and acquire the knowledge needed to sustain the growing national demand in the semiconductor industry, in line with the PERTE's interests and with a long-term vision.

To achieve this goal, a series of measures is proposed, as described below:

Firstly, a national network will be created for education, training and skills-building in relation to semiconductors, which universities, research centres and companies that are leaders in the semiconductor sector can join.

This network shall have an institutional alignment yet to be defined, with an effective, lean governance system in place and the necessary resources to be able to carry out the following functions, among others:

- Evaluating and quantifying training and skills-building gaps in relation to semiconductors and implementing structural measures to meet the staffing needs of the semiconductor industry.
- Developing different training, skills-building and advising activities as required by the industry, fostering the transfer of knowledge and the creation of companies.
- Launching a virtual platform used to spread knowledge among the design community, promoting cooperation between design companies, the scientific community, manufacturers of design tools and suppliers of intellectual property. This will provide non-discriminatory access to diverse libraries, innovative design tools and virtual prototyping[31].
- Offering companies and the scientific community access to the Spanish pilot lines, following a transparent, orderly procedure in coordination with other EU pilots and institutions.
- Raising awareness among the industry and other stakeholders about the need to strengthen the semiconductor sector and support it with the required knowledge, experience and capacities to bolster it.
- Providing information about the public aid instruments available to companies that approach the network, particularly SMEs.
- Facilitating the transfer of knowledge and experience among Member States.

Existing initiatives in this field, such as LOCA[32], the RISC-V Network[33], Quantum Spain[34], or Micronanofabs, as well as the Digital Innovation Hubs, may be used as reference for, or may be complemented by, the implementation of this action.

Secondly, a procedure will be developed for appointing candidates to join the European network of semiconductor competence centres provided in the European Chips Act. The chosen centre (or centres) will act as a liaison between the European network and the Spanish network in the terms established at EU level.

The measure will have an estimated budget of EUR 80 million for the 2022-2027 period.

31. 3D design, heterogeneous system architecture, integrated photonics, AI and quantum technologies, to name a few.
32. https://www.bsc.es/es/noticias/noticias-del-bsc/el-bsc-anuncia-el-inicio-de-una-colaboraci%C3%B3n-global-para-desarrollar-arquitecturas-de-computaci%C3%B3n-de
33. https://www.bsc.es/es/noticias/noticias-del-bsc/se-crea-la-red-riscv-para-impulsar-el-desarrollo-de-hardware-de-c%C3%B3digo-abierto
34. https://portal.mineco.gob.es/es-es/comunicacion/Paginas/211026_np_cuantico.aspx

3.3. COMPONENT THREE CONSTRUCTION OF FABRICATION PLANTS IN SPAIN

Reference framework

While Spain boasts a well-positioned scientific capacity in some key technologies, the national production capacity must be increased in the medium term so as to become aligned with the European goal of reaching 20% of global semiconductor production by 2030.

To this end, this component proposes two actions aimed at increasing Spain's production capacity: one aimed at manufacturing cutting edge technology, on a scale of less than 5 nm, and the other in the mid-range performance segment, greater than 5 nm.

Actions

Action 8. Creating fabrication capacity at sizes below 5 nm

The aim of this action is to create large-scale production capacity in Spain of cutting-edge semiconductors at sizes of less than 5nm, ideally in the foundry category, or one of its sub-segments[35].

In the first phase, a feasibility study will be conducted to analyse the suitability of developing the action in Spain, analysing the following aspects, among others:

- The sectors that could absorb the production, including domestic and international markets.
- Types of microchips and technologies that might be most successful.
- Identification of technology partners and potential investors.
- Detailed analysis of the value chain, including availability of minerals, chemicals and other critical supplies in Spain.
- Determining whether it would also be feasible to integrate the design and commercialisation phases, in addition to fabrication.
- Quantification of the most feasible investments, assessing financial, technical and staffing needs.
- Risk assessment, identifying technical, financial or labour limitations, among other constraints.
- Alignment with the framework of the EU European Chips Act.

In the second phase, building on the results of the feasibility study, the interest of possible stakeholders will be sought, and they will be asked to submit a highly detailed technical and financial business plan.

35. *Front-end* (fabricación de obleas), *back-end* (encapsulado, ensamblado y testeo) o ambas.

After analysing the proposals that best meet the interests of the PERTE, the most appropriate funding instrument shall be chosen that is compatible with state aid regulations in the European Union.

The action will have an estimated budget of EUR 7.25 billion for the 2022-2027 period.

A project of this magnitude can take up to 3 years to achieve the permits, engineering and construction (2022-2025), followed by 2 more years for commissioning and start-up (2026-2027). Ideally, the goal would be to have a plant in operation by late 2027, although the timelines could be adapted to the chosen projects.

Action 9. Creating fabrication capacity at sizes above 5 nm

The aim of this action is to create mass production capacity in Spain of mid-range performance semiconductors at sizes of more than 5nm, ideally in the foundry category, or one of its sub-segments.

In the preliminary phase, in conjunction with the previous Action, a feasibility study shall be conducted to determine which mid-range semiconductor fabrication technologies offer the greatest opportunity for development in Spain.

In light of the results attained, the interest of possible stakeholders will be sought, and they will be asked to submit a highly detailed technical and financial business plan.

After analysing the proposals that best meet the interests of the PERTE, the most appropriate funding instrument shall be chosen that is compatible with state aid regulations in the European Union.

The action will have an estimated budget of EUR 2.1 million for the 2022-2027 period.

As with the previous case, and following a similar timeline, ideally, the goal would be to have a plant in operation by late 2027.

3.4. COMPONENT FOUR STIMULATING THE ICT MANUFACTURING INDUSTRY IN SPAIN

Reference framework

The previous three components have outlined a series of measures aimed at intensifying the overall capacities of the semiconductor value chain, from the R&D&i phases through to microprocessor design and fabrication.

However, to supplement this, it is necessary, first of all, to understand the situation and level of integration of this value chain with a view to understanding its strengths and the sectors with the greatest carry-over effect in order to design tailored policies, but also the vulnerabilities that threaten the sustainability of the supply chain, so as to anticipate future semiconductor shortages.

Thus, a detailed report of the sector characteristics shall be drawn up in order to gain up-to-date insight on the semiconductor situation in Spain. Among other items, this report shall contain the following points:

- **Sector characteristics:** comparison with neighbouring countries and the main figures regarding turnover, employment, investment sources, exports, R&D expenditure, etc.
- **Map of R&D&i resources** including universities, pilot plants and leading technology centres in the field and renowned experts.
- **Industrial capacity map:** design, fabrication, commercialisation, equipment manufacturers, critical supplies, identifying key companies.
- **List of semiconductor usage as an intermediate input in the Spanish industry:** per usage sector, type of semiconductor used, country and company of origin.
- Identification of bottlenecks and production shortages in Spain.
- Risk assessment of the supply chain: Identifying factors that could alter semiconductor supply and demand. Among other factors, the risk factors identified by the European Commission[36] shall be taken into account.
- Other information of interest.

Secondly, in order to ensure that the semiconductor industry remains active, it is also vital to guarantee sufficient domestic demand in one of its natural consumer industries: the ICT manufacturing industry.

The ICT manufacturing sector is strong on imports, showing negative trade balances, especially with regard to the manufacturing of computers and peripherals, telecommunications equipment and consumer electronics, and strong dependence on Asia[37].

Creating new manufacturing capabilities in this country would help reverse this import trend while also having a significant carry-over effect on the sector as a whole.

Finally, it is necessary to continue focusing on innovation in a sector in which large numbers of start-ups are created but often cannot scale up due to shortages in the market, funding or opportunities in Spain, leading them to be sold to foreign entities or shut down.

Therefore, this issue must be addressed by creating a funding figure equivalent to the European Chips Fund[38], but adapting it to the specific needs of the Spanish semiconductor industry.

36. Recommendation (EU) 2022/210 on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem.
37. ONTSI, 2021. *Informe Anual del sector TIC, los medios y los servicios audiovisuales en España 2020.*
38. The European Chips Act envisages the creation of a chips fund to foster access to funding for start-ups and growing companies in the microelectronics sector, to be managed by Invest EU of the European Investment Bank (for loans and equity funds) and by the European Innovation Council (though its EIC Accelerator system).

Actions

Action 10. ICT manufacturing industry incentive scheme

The aim of this action is to bolster domestic production in the electronic product manufacturing industry (ICT manufacturing) so that it acts as a driving sector on the semiconductor industry and absorbs part of its production, either by installing new capacity or by enhancing the efficiency and competitiveness of existing plants.

The scope of application of the actions will extend to the ICT manufacturing industry[39] in the broadest sense, i.e., sectors that use microchips as an input for manufacturing electronic systems and equipment, telecommunications devices and consumer electronics (computers, tablets, digital cameras, etc.); but the focus may also be on attracting complex system manufacturing, which requires a sophisticated, highly integrated production ecosystem, such as in the case of personal computers.

This action will have a budget of EUR 200 million for the 2022-2027 period.

The chosen funding instrument may include the design of an integrated aid programme based on a series of measures for stimulating the value chain of the electronic product manufacturing industry, which would cover lines such as:

- Research, development and innovation line: for industrial research projects, experimental development, and innovation projects related to organisation and processes. Automation of production lines would be a special focus of this line.
- Sustainable innovation line: for investments that enable entities to increase the degree of environmental protection deriving from their activities beyond European Union standards or in absence of such standards.
- Energy efficiency innovation line: For innovative investments in energy savings or energy efficiency measures. Investments aimed at enhancements that lead to the achievement of higher energy efficiency levels in entities' production processes will be considered.
- Line of regional aid for investments. In assisted regions that meet the conditions stipulated in the 2022-2027 regional aid intensity map for Spain[40].

In addition, funding for larger investment volume projects may require the use of a specific line of regional incentives, separate from the integrated aid programme, in which the sector's specific funding needs would be laid out in an EOI.

This action will be carried out by the Ministry of Industry, Commerce and Tourism (MINCOTUR) in cooperation with the special commissioner for semiconductors.

39. Business Activity Code (CNAE) 26, possibly including other activities that are aligned with the interests of the PERTE.
40. https://ec.europa.eu/commission/presscorner/detail/es/ip_22_1763

Action 11. Creation of a chips fund

The aim of this action is to deploy a funding instrument for start-ups, scale-ups and other innovative SMEs in the Spanish semiconductor sector, helping them to shore up their positions in the domestic and European markets so as to reinforce the industrial fabric of the microelectronics industry.

Using the information in the sector-based report and other studies, technology lines that require strategic support will be identified: from design to fabrication, integration or ICT product manufacturing, which are aligned with the objectives of the PERTE.

The fund may offer diverse financing lines such as loans, equity interests, subsidies, venture capital or other types of financing tailored to the company's needs.

In particular, they may be set up at any of the entities that already manage funds, such as:

- Capital riesgo Innvierte (CDTI)
- Capital Riesgo Fondo Next Tech
- SEPIDES

In addition, efforts shall be made to align this fund with the Chips Fund envisaged in the European Chips Act.

The action will have a budget of EUR 200 million for the 2022-2027 period.

4. PERTE governance

This section outlines the governance system set up to ensure the coordination, effectiveness and consistency of the measures proposed in the PERTE.

The governance structures are described below:

Special Commissioner for Microelectronic and Semiconductors

This unit is responsible for promoting and coordinating all the PERTE's actions. The unit will have an executive and technical profile with a structure and level of representation that makes it possible to ensure the necessary recognition to carry out effective internal and external coordination that guarantees coherent, high-level dialogue with the industry.

Functions

The functions of the **Special Commissioner for Semiconductors** are detailed below, to be performed in coordination with the other competent administrative units:

a) Promoting and coordinating the development of the different actions involved in the PERTE.

b) Planning the PERTE's measures and coordinating the execution of actions for which ministerial bodies are responsible.

c) Establishing structured, permanent dialogue with the domestic and foreign industry to specify the PERTE›s actions, focusing especially on growing the fabrication and design capacity. All the above must be coordinated with existing structures in the administration.

d) Assessing the technical and financial feasibility of proposals for constructing fabrication plants in Spain and also proposals for setting up fabless companies.

e) Preparing and coordinating the state aid notification processes that may be developed in the framework of the European Chips Act ("integrated production facilities" or "EU open foundries").

f) Assisting in setting up European consortiums as deemed necessary for the purpose of applying for projects in the Pillar I Chips for Europe initiative.

g) Preparing and coordinating the fast-tracking procedures relating to the planning, construction and operation of chips fabrication plants that may be established in the European Chips Act, and acting as a Single Point of Contact. To this end, a channel of dialogue will be established with the autonomous communities and municipalities for all matters related to environmental, zoning and other permits.

h) Acting as the representative in the governance structure envisaged in the European Chips Act, in particular on the *European Semiconductor Board*, or the European Semiconductor Expert Group (transitional group) or, where appropriate, assisting the unit acting as representative.

i) Acting as the representative to the European Alliance on Processors and Semiconductor Technologies, in the part reserved for the institutional sector, or assisting the unit acting as representative.

j) Other actions required to achieve the objectives of the PERTE.

The structure

The Special Commissioner for Semiconductors shall be structured as follows:

- **Special Commissioner for Semiconductors.** A highly reputable individual with a professional background in the microelectronics and semiconductor sector will be appointed, ideally someone with previous experience in management positions at a large company and academic training in this field. This person will be the public face of the unit and will receive the institutional support required to coordinate the national position and maintain high level dialogue under a unified voice with the industry.
- **Commissioner's technical office.** The Technical Office will support the Commissioner in the performance of the functions assigned to such party and will have access to staff and resources to achieve the objectives of the PERTE. It will receive support from the common services of the organisation it belongs to and from the other ministries with executive responsibilities in the PERTE.

Inter-Ministry Working Group

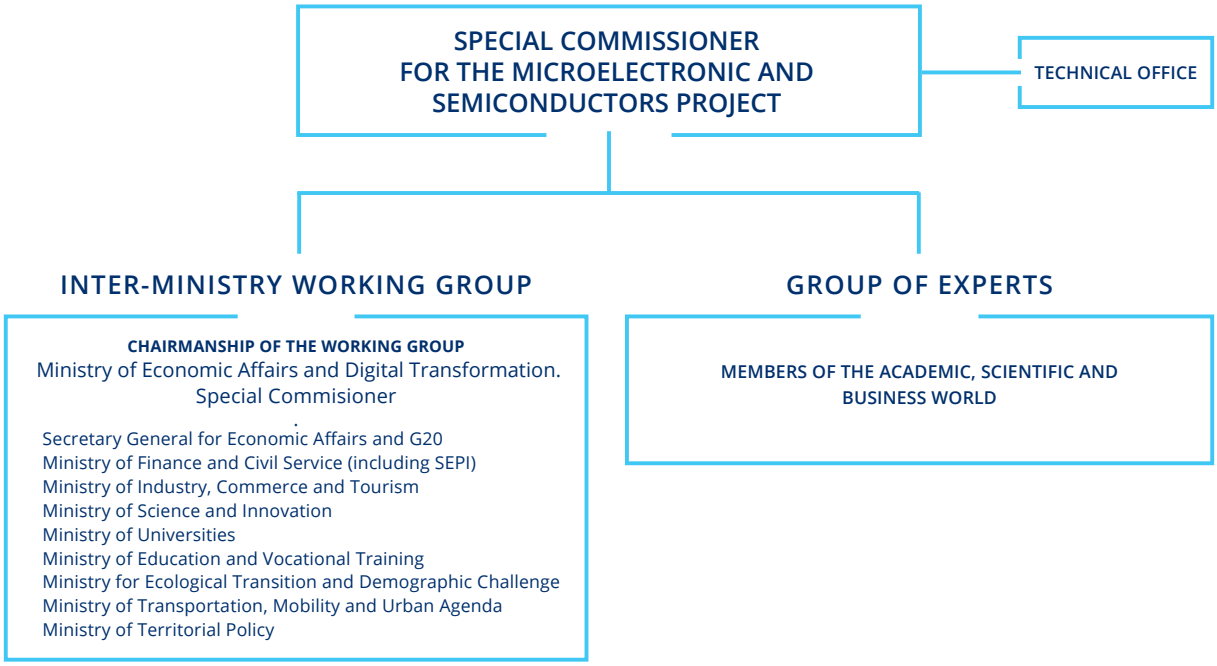
The Inter-Ministry Working Group is the decision-making and coordination body, consisting of representatives from the competent ministry departments related to the actions carried out under the PERTE Chip, with the aim of performing joint operational monitoring of the planned execution instruments.

The Inter-Ministry Working Group will be chaired by the Ministry of Economic affairs and Digital Transformation.

Group of experts

A Group of experts will be convened to act as an advisory body comprising diverse experts that are leaders in the academic, scientific and business worlds in the field of semiconductors[41].

This Group of experts will provide information and strategic guidance, harnessing their knowledge of the sector with a view to further defining the PERTE actions and maximising their impact, both in the field of R&D&i and in design and fabrication.



41. A modo de referencia, el congreso *Design of Circuits and Integrated Systems (DCIS)* reúne a una impórtate comunidad científica de referencia en la materia. Lo mismo ocurre con la *Photonic Integration Week* en el caso de la fotónica integrada.

5. Instruments

The measures envisaged in the PERTE shall be implemented through diverse management instruments. Each organisation involved shall assess these instruments and their adequacy within the procedural framework and the established timeline.

Based on the needs that arise, studies, consultations and expressions of interest or other formulas shall be used as deemed appropriate to define the field of action and the requirements of the different actions, following the guidelines established in this PERTE.

Diverse public-private or inter-administrative cooperation agreements can also be reached if this is considered necessary for the execution of the PERTE, including eventual involvement in Joint Undertakings or European consortia

In all cases, the conditions, calls for proposals, contracts, commissions and other financial instruments must comply with the framework for state aid of the European Union.

Specifically, an alignment with the objectives and procedures of the European Chips Act shall be sought.

In this regard, efforts shall be made to align, or integrate, where appropriate, the actions related to R&D&i, design, pilot lines and the chips fund with the objectives of the Chips for Europe initiative of Pillar I, particularly with the actions developed under the envisaged Chips Joint Undertaking and its future work programmes.

In turn, the actions designed to increase fabrication capacity could be adjusted to the terms of Pillars II and III of the European Chips Act, adapting, where appropriate, to the concept of the "first-of-a-kind facility in the Union" as "Integrated Production Facilities"[42] or "Open EU Foundries", so as to increase the public aid options or to streamline administrative procedures, but also assigning certain conditions in terms of security of supply.

At any rate, all references to the European Chips Act could be subject to a certain degree of variation as the legislative negotiations progress within the European Union institutions[43]. However, it is worth noting that the Commission indicates in its Communication "A Chips Act for Europe" that the criteria of the proposed European Chips Act will be taken into account for those notifications initiated prior to the adoption of the regulation by the Parliament and the Council, with the expectation of formal recognition once the Act enters into force[44].

42. Fabless component may be integrated with fabrication components, in this case.
43. The European Chips Act is still in the legislative proposal phase and is currently under negotiation. https://oeil.secure.europarl.europa.eu/oeil/popups/ficheprocedure.do?reference=2022/0032(COD)&l=en
44. COM(2022) 45 A Chips Act for Europe. *"For projects for which State aid is notified before the proposed Chips Act is adopted, the Commission will take into account their compliance with the criteria for Open EU Foundries and Integrated Production Facilities as set out in the proposed Chips Act with the expectation that such projects would apply for formal recognition once the Chips Act enters into force."*

Additionally, as previously mentioned, these will be subject to certain degree of flexibility so as to orient the actions as the project progresses, within reasonable margins of technological uncertainty.

Finally, the applicable regulations of the Recovery and Resilience Facility and its guidelines[45], shall be followed, as well as the terms of the Recovery, Transformation and Resilience Plan and Royal Decree-Law 36/2020.

45. SWD(2021) 12 final. https://ec.europa.eu/info/sites/default/files/document_travail_service_part1_v2_en.pdf

6. Budget and execution

A total investment of EUR 12.25 billion has been allocated to the PERTE Chip, to be executed through a number of organisations and financial instruments. The following sections provide information about the execution of the actions and their multi-year breakdown.

The main source of financing will come from the addenda to the recovery plan, and will be subject certain variability and conditioned to the final approval by the Commission.

6.1. Detailed budget

COMPONENTS	EXECUTION*	FUNDING	NATURE	INSTRUMENTS	BUDGET M€
COMPONENT ONE - BOLSTERING SCIENTIFIC CAPACITY					**1,165**
ACTION 1. Development of R&D&i on alternative architecture microprocessors	MCINN, MINECO	RTRP addendum	Transfer (grant)	Grant	475
ACTION 2. Development of R&D&i on integrated photonics	MCINN, MINECO	RTRP addendum	Transfer (grant)	Grant	150
ACTION 3. Development of R&D&i on quantum chip development	MINECO-SEDIA	RTRP addendum	Transfer (grant)	Grant	40
ACTION 4. Budget line for the IPCEI on Micro-electronics and communication Technologies	MINCOTUR, MINECO	C12.I2 - C15.I5 RTRP addendum	Transfer (grant)	Grant	500
COMPONENT TWO - DESIGN STRATEGY					**1,330**
ACTION 5. Creation of fabless alternative architecture microprocessor design companies	MINECO, MINCOTUR, COMMISSIONER	RTRP addendum	Capital contribution	Contract or commission, EOI, capital contribution	950
ACTION 6. Creation of test pilot lines	MINECO, MINCOTUR COMMISSIONER	RTRP addendum	Transfer (grant)	Grant	300
ACTION 7. Creation of a network for education, training and skills-building in relation to semiconductors	MCINN, MINECO, UNIVERSITIES, EDUCATION	RTRP addendum	Transfer (grant)	Agreement, commission, grant, others	80
COMPONENT THREE - CONSTRUCTION OF FABRICATION PLANTS IN SPAIN					**9,350**
ACTION 8. Creating fabrication capacity at sizes below 5 nm	COMMISSIONER, INTER-MINISTRY GROUP	RTRP addendum	Capital contribution	Contract or commission, EOI, capital contribution	7,250
ACTION 9. Creating fabrication capacity at sizes above 5 nm	COMMISSIONER, INTER-MINISTRY GROUP	RTRP addendum	Capital contribution	Contract or commission, EOI, capital contribution	2,100
COMPONENT FOUR - STIMULATING THE ICT MANUFACTURING INDUSTRY IN SPAIN					**400**
ACTION 10. ICT manufacturing industry incentive scheme	MINCOTUR	RTRP addendum	Transfer (grant)	Grant or loans (conditions order)	200
ACTION 11. Creation of a chips fund	MCINN, MINECO, COMMISSIONER	RTRP addendum	Capital contribution	Venture capital fund contribution	200
GOVERNANCE					**5**
Special Commissioner for Semiconductors	MINECO	RTRP addendum	Chapter 8		5
TOTAL PERTE CHIP BUDGET					**12,250**

*** Acronyms: MCINN:** Ministerio de Ciencia e Innovación (Ministry of Science and Innovation). **MINECO:** Ministerio de Asuntos Económicos y Transformación Digital (Ministry of Economic Affairs and Digital Transformation). **SEDIA:** Secretaría de Estado de Digitalización e Inteligencia Artificial (Secretary of State of Digitization and Artificial Intelligence). **MINCOTUR:** Ministerio de Industria, Comercio y Turismo (Ministry of industry, trade and tourism). **COMMISSIONER:** Special Commissioner for the Microelectronic and Semiconductors Project. **UNIVERSITIES**: Ministerio de Universidades (Ministry of Universities). **EDUCATION:** Ministerio de Educación y Formación Profesional (Ministry of Education and Vocational Training). **INTER-MINISTR G.:** Inter-Ministry Working Group.

NOTE 1. Actions 5, 8 and 9 take into account the need to reserve 1% of the total budget to carry out actions related to the management of projects like feasibility studies, reports, legal consulting, funding studies, impact assessments, selection of plots of land and others.

NOTE 2. Actions 8 and 9 could be supplemented, based on the needs, with an ad hoc line of regional incentives (Law 50/85).

6.2. Multi-year budget breakdown

COMPONENTS	2022	2023	2024	2025	2026	2027	BUDGET M€
COMPONENT ONE BOLSTERING SCIENTIFIC CAPACITY	**250**	**340**	**285**	**170**	**120**		**1,165**
ACTION 1. Development of R&D&i on alternative architecture microprocessors		115	130	140	90		475
ACTION 2. Development of R&D&i on integrated photonics		55	35	30	30		150
ACTION 3. Development of R&D&i on quantum chip development		20	20				40
ACTION 4. Budget line for the IPCEI on Microelectronics and communication Technologies	250	150	100				500
COMPONENT TWO DESIGN STRATEGY		**230**	**350**	**400**	**350**		**1,330**
ACTION 5. Creation of fabless alternative architecture microprocessor design companies		150	250	300	250		950
ACTION 6. Creation of test pilot lines		60	80	80	80		300
ACTION 7. Creation of a network for education, training and skills-building in relation to semiconductors		20	20	20	20		80
COMPONENT THREE CONSTRUCTION OF FABRICATION PLANTS IN SPAIN		**684**	**1,596**	**2,509**	**3,421**	**1,140**	**9,350**
ACTION 8. Creating fabrication capacity at sizes above 5 nm		530	1,238	1,945	2,652	884	7,250
ACTION 9. Creating fabrication capacity at sizes above 5 nm		154	359	563	768	256	2,100
COMPONENT FOUR - STIMULATING THE ICT MANUFACTURING INDUSTRY IN SPAIN		**130**	**110**	**90**	**70**		**9,350**
ACTION 10. ICT manufacturing industry incentive scheme		80	60	40	20		200
ACTION 11. Creation of a chips fund		50	50	50	50		200
GOVERNANCE		**1**	**1**	**1**	**0.5**	**0.5**	**5**
Special Commissioner for Semiconductors		1	1	1	0.5	0.5	5
TOTAL PERTE CHIP BUDGET							**12,250**

7. Initiative requirements

7.1. Requirements of the Recovery, Transformation and Resilience Plan

The PERTE on microelectronics and semiconductors (PERTE Chip) meets the objectives of the Recovery and Resilience Facility established in article 3 of Regulation (EU) 2021/241 of the European Parliament and of the Council of 12 February 2021 establishing the Recovery and Resilience Facility (RRF Regulation).

This section assesses the overall contribution of the PERTE to the six pillars set out in the Recovery, Transformation and Resilience Plan. Furthermore, the PERTE does not cause significant harm, following one of the horizontal principles affecting all the funds of the Recovery and Resilience Facility.

7.1.1. Contribution to the ecological transition

The PERTE Chip addresses the entire value chain of semiconductors, microelectronics and ICT manufacturing from a comprehensive viewpoint to achieve greater efficiency in its processes, thus contributing to the ecological transition of the economy through the use of more sustainable technologies and digital services.

Semiconductors, as essential enablers of digitalisation, are fundamental to the ecological transition and the achievement of energy and climate goals, playing a decisive role in the road toward climate neutrality. This is set out in the Strategic Energy and Climate Framework, which is composed of diverse strategic and legislative elements such as Law 7/2021, of 20 May, on Climate Change and the Energy Transition, the Integrated National Energy and Climate Plan (PNIEC) 2021-2030, the Just Transition Strategy, and the 2050 Long-Term Decarbonisation Strategy.

This capacity as a natural enabler of climate neutrality is also reflected in the fact that this activity is not included in the Emissions Trading System.

At any rate, the procedures that could arise as a result of the "Do no significant harm" principle (DNSH) shall be assumed to apply to the fabrication and ICT manufacturing activities included in this PERTE, seeking an alignment with the conditions to be established in the European Chips Act.

Having considered the above, compliance with the DNSH principle is outlined below:

"Do no significant harm" principle

Pursuant to the terms of the Recovery Plan, Regulation (EU) 2021/241 of the European Parliament and of the Council, of 12 February 2021 establishing the Recovery and Resilience Facility, and its implementing regulations, particularly Commission Notice (2021/C 58/01) Technical guidance on the application of the 'do no significant harm' principle, and the requirements of the Council Implementing Decision on the approval

of the assessment of the Recovery, Transformation and Resilience Plan for Spain (CID) and its Annex document, all the actions to be performed in accordance with this PERTE that are funded by the Recovery and Resilience Facility must obey the principle of not causing significant harm to the environment. This includes compliance with any specifically assigned conditions that may apply to the measures under which the actions are to be taken, especially those outlined in the document of each Component of the Plan and in the Annex to the CID.

The requirements to be met in order to align the project with the European "Do no significant harm" principle are as follows:

Climate change mitigation

The project does not give rise to considerable greenhouse gas emissions for the following reasons:

First of all, as an activity aligned with the European Chips Act, its aim is to design and produce high-performance, cutting-edge chips with highly energy-efficient processing.

Following this approach, even if foundries for more mature technologies are built, this will still contribute to reducing greenhouse gases on a global level: on the one hand, because they must comply with EU environmental regulations, which are much stricter than the standards in the countries where production currently takes place, and on the other, by considerably reducing the transportation needs between each of the steps of fabrication and subsequent transfer to Europe[46].

In addition, the fact that the chips designed are intended for use in alternative architectures such as reduced instruction sets with an open approach (RISC-V) renders them not only more efficient but also increases their possibilities for use as general-purpose processors, thus expanding the versatility of destination sectors, including data centres, telecommunications networks, Artificial Intelligence and connected, electric vehicles, ultimately leading to greater data processing optimisation and decreasing energy consumption. This is also replicable in the medium and long term to technologies like integrated photonics and quantum chips, which will offer greater computing capacity through more efficient processes.

In this regard, it is worth mentioning the direct contribution to the targets of the "Fit for 55" package of proposals focused on promoting cleaner vehicles and cleaner fuels in compliance with the climate goals for 2030 on the road to climate neutrality . It should be noted that this PERTE will directly contribute to the use of more efficient

46. For example, in the process of manufacturing a smartphone, the wafers are fabricated in Taiwan, dicing, testing and packaging takes place in Malaysia, the chip is integrated with other electronic components of the smartphone in China and then it is transported to the West for physical sale, all by means of maritime transportation, which normally causes pollution. If fabrication is relocated to Europe, both the transportation needs and the resources used will be reduced, and road transport options using alternative fuels or more efficient transport methods like freight trains can be used. Source: April 2021, "Strengthening the semiconductor supply chain in an uncertain era", Boston Consulting and SIA (Semiconductor Industry Association). https://www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf

microprocessors and designs that could be used in connected and electric vehicles, in both their instrumentation and connectivity sub-systems and in the 5G networks that will enable their mass deployment.

Finally, in the field of design and installation of test pilots, the PERTE aims to develop the use of techniques that enable more efficient, low consumption designs through advanced fabrication processes such as 3D design and heterogeneous system architecture. The design platform open to the scientific community and the deployment of new pilots will make it possible to fabricate and validate the first chip prototypes in Spain or Europe, freeing them from the need to seek out test lines at foundries located in Asia. All of this cuts validation costs, reduces intervals between design phases, especially for SMEs, and accelerates innovation in microchip design overall.

Climate change adaptation

For the purpose of determining whether the PERTE Chip actions will lead to an increase in the adverse effects of current and expected climate conditions on climate itself, on individuals, nature or the assets, an assessment will be made of the vulnerabilities and physical climate risks of the activity, the quantification of its impact and the possible adaptation solutions to deal with them, following the principles and requirements set out in the Delegated Act on Taxonomy for climate goals. This assessment shall be consistent with the scale of the activity, its expected duration and its possible impacts.

Sustainable use and protection of water and marine resources

The risks of environmental degradation related to the preservation of water quality and prevention of water stress will be determined and addressed with the aim of achieving good ecological status and good ecological potential of water as defined in article 2, points 22 and 23 of Regulation (EU) 2020/852, pursuant to Directive 2000/60/EC of the European Parliament and of the Council (Water Framework Directive). A water protection and usage management plan shall also be prepared for the potentially affected water mass or masses, in consultation with the relevant stakeholders.

If an environmental impact analysis has been conducted in accordance with Law 21/2013, of 9 December, on environmental assessment, that includes an analysis of the impact on water pursuant to the Water Framework Directive, no additional analyses shall be required, as long as the risks identified have been addressed.

Transition to a circular economy, including waste prevention and recycling

With a view to ensuring that the PERTE actions contribute to the transition to a circular economy, the criteria set out in the Delegated Act on Taxonomy for climate goals shall be followed. In particular, an alignment may be sought with the enabling technologies described in point 3.6 of the Annex as “Manufacture of other low carbon technologies”, in addition to following other generic criteria established in said delegated act that may apply.

In this regard, certain aspects of the PERTE Chip that directly contribute to the circular economy must be mentioned here, such as advance microprocessor packaging and assembly technologies, enhanced efficiency through the use of lighter-weight architecture and the use of other new chip design techniques mentioned throughout this report.

Finally, the initiative is also aligned with the Circular Economy Plan, which identifies electronics and ICTs as a value chain in which designs are to be enhanced to adopt energy efficiency and durability, reparability, upgradability, maintenance, reuse and recycling criteria, in accordance with the Ecodesign Directive[47].

Pollution prevention and control

The PERTE Chip has a strong tendency to facilitate the ecological transition and it is not expected to cause a significant increase in polluting emissions into the atmosphere, water or soil.

However, the general criteria relating to the principle of doing no significant harm may be applied to pollution prevention and control in relation to the use and presence of chemicals established in Appendix C of Annex I of the Delegated Act on Taxonomy for climate goals.

Protection and restoration of biodiversity and ecosystems

It shall be ensured that the manufacturing plants have no negative effect on biodiversity and ecosystems. Thus, where required and in line with the criteria set out in the European Chips Act, an environmental impact assessment shall be completed in accordance with the terms of Law 21/2013, of 9 December, on environmental assessment.

After analysing the six DNSH principles in general, each action linked to the development of the PERTE shall explicitly include the specific DNSH conditions that apply, in accordance with the documentation for the Component to which they belong, and any other conditions taken from the CID for the relevant investment or reform, as appropriate.

7.1.2. Contribution to the digital transition

As indicated throughout the report, semiconductors are an essential, basic component of the digitalisation of our society and for this reason, the PERTE Chip unequivocally contributes to the digital transition in an aggregate manner.

However, it is worth highlighting its clear alignment with the EU's digital policies in general, such as the Communication about the Digital Decade, which establishes the EU's four strategic digitalisation goals, or the proposed Decision establishing the 2030 policy programme "Path to the Digital Decade", which, together with the European Chips Act, will establish the measures for achieving those goals.

47. COM(2020) 98 final, 11.03.2020.

On a domestic level, the PERTE Chip contributes to the achievement of the 2025 Digital Spain goals and to the development of all its strategic plans.

Finally, it will generate a ripple effect on all the digitalisation actions of the different components of the Recovery, Transformation and Resilience Plan.

7.1.3. Contribution to social and territorial cohesion (impact on the territory)

Given the integrated, cross-disciplinary nature of the PERTE actions, the plan will contribute to social cohesion by promoting the deployment of digital services overall.

More specifically, the PERTE is aligned with the key elements of government policy, having an added, evenly distributed effect on the territory.

In this regard, it must be noted that Spain's semiconductor value chain is spread throughout the country, beyond the leading technology hubs. This feature acts as a safeguard to ensure a proportionate impact across the country. In addition, these effects are increased by the driving sectors, particularly the automotive sector and the components industry, which have plants located all over Spain.

7.1.4. Contribution to gender equality

The PERTE contributes to gender equality policies by stimulating the long-term job market for technical positions, particularly those in the STEM branches. According to data from the National Observatory of Telecommunications and the Information Society (ONTSI), the number of women employed in the ICT sector is increasing in absolute terms[48].

7.1.5. Contribution to other horizontal principles

Finally, this PERTE chip comply with other horizontal principles set in the Recovery and Resilience Facility, such as fraud and conflicts prevention, double financing or meeting state aid rules.

The implementing instruments will include measures to meet the abovementioned.

7.2. Compliance with the requirements of RDL 36/2020

For all the reasons outlined throughout this descriptive report, the PERTE Chip can clearly be classified within the priorities envisaged in the Recovery, Transformation and Resilience Plan. It also meets all the criteria required to be declared a Strategic Project for Economic Recovery and Transformation (PERTE), in virtue of Royal Decree-Law 36/2020:

1. ***It poses an important contribution to economic growth, the creation of jobs and the competitiveness of the Spanish industry and economy, bearing in mind its positive carry-over effects on the domestic market and on society.***

48. Breakdown of the number of employees per gender in the ICT sector (2018) https://www.ontsi.es/sites/ontsi/files/2019-12/InformeAnualSectorTICC2019.pdf

The proposed PERTE is aimed at the Spanish economy as a whole thanks to the cross-disciplinary nature of its actions, but it has a clear, direct impact on research, development and innovation activities and on the manufacturing industry in general.

Among the sectors on which the PERTE will have the greatest impact is the automotive industry, a highly strategic industry with a strong carry-over effect on the economy as a whole, which employs more than 2.5 million people (between direct and indirect jobs) and plays a significant part in the national GDP, with companies distributed throughout the whole of Spain[49].

However, the sector in which the most disruptive changes will occur is the ICT manufacturing industry, which will once again have the capacity to manufacture semiconductors on a commercial scale. This phenomenon will act as a catalyst on the domestic semiconductor value chain overall, generating positive cross-sector effects for suppliers of raw materials and specialised equipment as well as in direct consumer sectors like electronic equipment manufacturing, the automotive industry, telecommunications and other technology-related assets.

2. ***It makes it possible to combine knowledge, experience, financial resources and economic stakeholders for the purpose of filling important gaps in the market or systemic shortcomings and social challenges that could not otherwise be addressed.***

Spain and the European Union are currently in the midst of a strategic transformation process aimed at the creation of a more ecological, digitalised and resilient economy. However, the semiconductor sector is a complex sector in which there are a number of market weaknesses, such as high entry barriers, geographic concentration and the inelasticity of supply, which can prompt significant shortage crises that place a burden on the EU's competitiveness.

This means that a change in the production model for this unique industry is not without its risks, so it could scarcely be carried out without resolute support from the government. Therefore, the proposed project aims to resolve these market weaknesses by offering the sector an appropriate environment in which, based on the sector's strengths and through the collaboration of all its stakeholders, important investments can successfully be made and projects can be implemented that are transformative for the entire value chain of the microelectronics and semiconductor industry.

3. ***It has an important innovative nature and provides significant added value in terms of R&D&i, by enabling the development of new products, services or production processes, for example.***

The PERTE Chip is based on the pronounced innovative nature of its actions, starting with its first component devoted exclusively to R&D&i, followed by a second component

49. PERTE VEC https://www.mincotur.gob.es/es-es/recuperacion-transformacion-resiliencia/perte/memoria-descriptiva-perte-vec.pdf

that capitalises on the scientific achievements to promote innovative microchip design companies, then moving on to an ambitious third component in which this progress is materialised in the actual fabrication of high-performance semiconductors, as a first-of-a-kind in Spain.

The project is completed with a fourth component that aims to keep the characteristic focus on innovation in the sector, foreseeably generating a ripple effect in scientific activity, given that the electronics industry is one of the most R&D and innovation-intensive industries[50].

4. It is quantitatively and qualitatively important, with a particularly large size or scope, and it poses a very high technological or financial risk.

This PERTE Chip represents a change of paradigm for the microelectronics and semiconductor sector in Spain which is only possible through the coordinated mobilisation of significant investments in the field of R&D&i, design and fabrication.

As indicated in this report, the magnitude of the investments needed to build a cutting-edge technology foundry could exceed EUR 15,000 million. This volume of capital entails a very high financial and technological risk, so it is essential to have accompaniment and support from the administration throughout the entire investment process.

5. It encourages the integration and growth of small and medium enterprises and promotes collaborative environments.

Cooperation is one of the inspirational principles of the PERTE and is an essential tool for achieving its objectives. The actions foreseen would not be possible without cooperation between companies, research centres and other industry stakeholders.

Furthermore, the PERTE specifically envisages the creation of a collaborative setting in which small and medium enterprises have access to and can share resources to bolster their competitiveness, in addition to allocating a specific amount to strengthen the entrepreneurial ecosystem of the sector through the chips fund.

6. It contributes in a specific, clear and identifiable manner to one or more of the objectives of the Recovery, Transformation and Resilience Plan for the Spanish Economy, particularly as regards the targets set at European level in relation to the European Recovery Instrument.

The PERTE Chip contributes specifically to several of the general objectives defined in the Recovery, Transformation and Resilience Plan, most notably:

- **Promoting the digital transformation,** an objective to which it unequivocally contributes due to the very nature of semiconductors.

50. Presentaciones Sectoriales 2021 (MINCOTUR). https://www.mincotur.gob.es/es-es/IndicadoresyEstadisticas/Presentaciones%20sectoriales/00.%20Total%20Industria.pdf

- **Smart, sustainable and inclusive growth, including economic cohesion, employment, productivity, competitiveness, research, development and innovation and proper functioning of the internal market with strong SMEs.** The series of actions in the PERTE Chip are aimed at generating sustainable, innovative and long-lasting structural growth in the microelectronics and semiconductor industry that will aid in consolidating an ecosystem of highly competitive large corporations and SMEs.

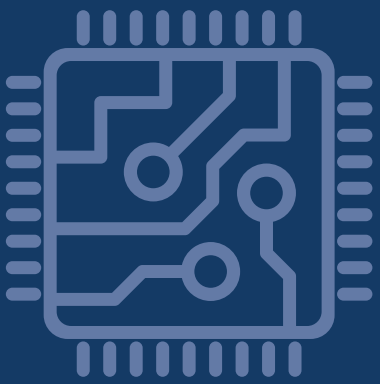
7. Finally, it should be highlighted that this PERTE does not distort effective market competition.

The actions included in this PERTE Chip do not distort effective market competition. The design and functioning of the actions shall follow the principles of transparency and non-discrimination, promoting participation amongst all the economic stakeholders that are interested in participating and that meet the requirements established for each of the support instruments.

To this end, the instrument design shall pay special attention to compliance with state aid regulations, with article 101 of the Treaty on the Functioning of the European Union and with Competition Law 15/2007, of 3 July, in relation to anti-competitive agreements.

Specifically, the lines of support for fabrication or design can be notified as state aid for the purposes of declaring their compatibility pursuant to article 107.3 of the Treaty on the Functioning of the European Union and, particularly, seeking an alignment with the European Chips Act. Any aid granted in this regard is subject to express authorisation from the European Commission.

Recovery,
Transformation and
Resilience Plan



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