Neuromorphic Technology Insights in Spain

Invited Paper

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***Abstract*—This paper provides an overview of the main research activities carried out by Spanish organizations in areas related to neuromorphic technologies, spanning physical, materials, circuitry, and architectural levels. It also discusses the potential of these technologies to create competitive advantages for the Spanish industry, and to foster new applications and business opportunities via deep-tech startups – especially related to novel neuromorphic sensing modalities (e.g., Dynamic Vision Sensors).**

I. Introduction

In 2022, the Spanish Government launched the PERTE Chip program to bolster the design and production capabilities of electronics chips in Spain [1]. Its four main objectives are: (1) Boost Spanish scientific capabilities, (2) Strengthen Spanish fabless design strategy, (3) Build chip manufacturing plants in Spain, and (4) Stimulate the Spanish ICT industry by funding SMEs and startups in the semiconductor sector. The PERTE Chip will invest 12,250 million euros between 2022 and 2027, running in liaison with the EU Chips Act. We posit that emerging neuromorphic technology offers good opportunities to address the objectives of the PERTE Chip (and EU Chips Act), building on research results and initiatives ongoing at Spanish organizations, which are outlined in this paper.

A. Neuromorphic Technology and Open Challenges

Neuromorphic technologies seek to replicate the brain's mechanisms for processing information through microelectronics and/or photonics designs with unprecedented levels of performance (e.g., ultra-low processing latency) and energy efficiency [2]. Neuromorphic technologies are considered a 'critical enabler' for the development of the 3^{rd} AI generation [3] – more capable than its predecessors, bringing support for on-device online adaptation and learning. In recent years, there has been a surge in startups commercializing neuromorphic chips, complementing the efforts of established corporations such as Intel, IBM, HP, Qualcomm, and Samsung in advancing this technology. Notably, Yole forecasts that neuromorphic chips – sensors and processors – will account for 18% of the global AI chip market by 2035, capturing a segment worth an estimated 20 USD billion [4].

Neuromorphic vision sensors (e.g., Prophesee) are inspired by the way light is sensed in biological retinas. As opposed to frame-based vision sensors, neuromorphic Dynamic Vision Sensors (DVS) sense surroundings in a continuous manner, Each DVS pixel operates independently and asynchronously and generates visual events when its brightness change surpasses a configurable threshold. Hence, generating a flow of visual events that encode a spatiotemporal representation of the visual reality with extremely high temporal resolution (eq. to 1,000 fps) [5]. This allows to capture very fast motions without suffering from motion blur, which is typical in frame-based sensors. Moreover, the data volume produced by DVS compares very favorably with regular full frames that include much redundant data. This translates into lower energy consumption and shorter latency, especially where the sparseness of the event output is leveraged by processing paradigms, such as event-driven Spiking Neural Networks (SNNs) [6].

Unlike mainstream 2^{nd} generation of AI processors, which are optimized to process vast amounts of data regardless of their information value (e.g., GPUs), *neuromorphic processors* run SNNs to process only high-information value data (e.g., visual events) with extremely low latency and high energy-efficiency – orders of magnitude better than mainstream GPUs [7]. Namely, neuromorphic processors typically implement parallel dataflow architectures driven by incoming sensor events and spikes produced by firing (biologically plausible) neurons, avoiding the continuous back-and-forth transfers of data (and instructions) with memory in 2^{nd} AI generation processors as they run neural networks in a layer-after-layer sequential mode. However, as neuromorphic chips typically implement neurons in dedicated silicon to improve energy efficiency and latency, an important limitation is the size of the SNNs they can run, which is restricted by the implemented neuron count. Most commercial neuromorphic processors, such as Innatera and Synsense, can run only relatively simple SNNs (e.g., audio) whereas BrainChip, Intel Loihi, and IBM TrueNorth can run sufficiently large vision SNNs.

Novel materials, devices, and implementation approaches are being explored using photonics, analog and in-memory computing to overcome the challenges of mainstream CMOS process technology and create more area- and energy-efficient neuromorphic chips.

At the *circuit level*, memristive technology is becoming one of the most promising alternatives [8], combining CMOS with nano-scale devices. However, the current technical limitations of memristors impede the development of compact dense memristive chips. Presently, there are hybrid fabrication technologies, like the one provided by STMicroelectronics on 130-nm process node which includes the OxRAM post-process from CEA-LETI to fabricate memristors as embedded Non-Volatile Memory (NVM) devices [9]. This technology uses filamentary HfOx memristors which require an initial forming step where a high-voltage is applied while limiting the maximum current flowing through the device. This current is limited by an nMOS transistor connected in series to the memristive device, building a 1T1R structure, and therefore consuming CMOS area for each memristor, which in turn reduces the density of these nanodevices.

A wide range of novel *materials* is currently on active research to enhance or surpass the neuromorphic functionalities of memristors. Among them, Spintronic materials [10], which can manipulate both charge and spin degrees of freedom of electrons, have emerged as promising candidates for implementing non-volatile memristive devices [11], as well as binary memory devices (Magnetic Random Access Memories, MRAMs) [12], logic operations in circuits [13], high-frequency detectors (Spin Diodes) and sources (Spin Hall Nano oscillators) at the nanoscale [14].

At the *application/algorithmic level*, novel training techniques for SNNs are starting to overcome the difficulties of training large event-based networks (e.g., surrogate gradient backpropagation [15] and eligibility traces approaches [16]). However, for some applications they still suffer from the vanishing gradient problem and are computationally intense. Neuromorphic AI is also providing interesting outputs in optimization and control [17], [18]. Besides, SNNs can encode far more information than 2^{nd} AI generation networks as they operate in the spatiotemporal domain using spikes.

Sections II to V in this paper cover the ongoing research activities in Spain at various levels: materials and devices, circuits, sensors, and processing architectures. Section VI focuses on applications, and Section VII discusses the perspectives for technology adoption and its potential impact on the industry.

B. Overall Context in Spain

To bring together the activities of the main Spanish research centers and universities in the areas related to neuromorphic technologies introduced above, and to align these with the interests of the industry, we have created a *Working Group on Neuromorphic and AI Technologies* within the Spanish Semiconductor Industry Association (AESEMI) [19]. Fig. 1 shows the location, technology and application sector of the Spanish organizations covered in this paper.

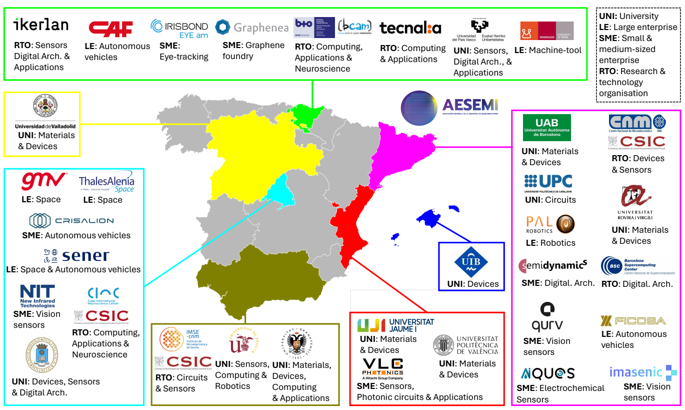

Fig. 1. Location and expertise of organizations covered in this paper.

II. Materials and Devices

Fig. 2 shows the organizations and technologies related to neuromorphic materials and devices in Spain.

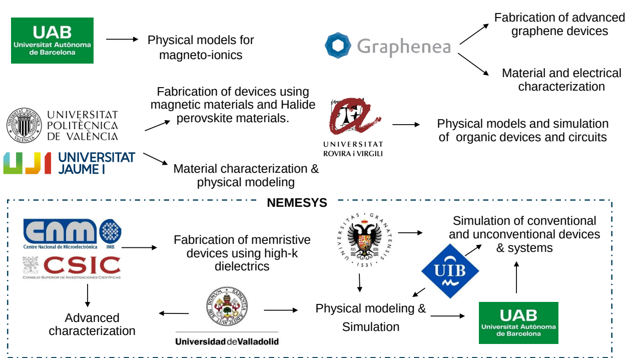

Fig. 2. Neuromorphic materials and devices in Spain.

The Universitat Jaume I (UJI) is exploring the implementation of mem-computing paradigms [20] using *magnetic materials* with novel properties, and *Halide perovskite materials*, which have been at the front of investigations of high-performance memory, photovoltaic and optoelectronic devices.

UJI's research on Spintronic devices for neuromorphic applications (driven by the SPINAD lab directed by Dr. Victor Lopez) is focused on devices based on *antiferromagnetic materials (AFM)* [21] due to their zero-net magnetization (offering superior scalability than ferromagnets) and their picosecond dynamics [22]. For example, they have been proposed as a candidate to store synaptic weighs at the nanoscale (through the dynamics of their magnetic domains of 2 nm in size) that results in a scalable technology. UJI has demonstrated the analog resistance behavior of antiferromagnetic micropillars and nanopillars (with diameters ranging from 10 μm to 800 nm diameter) consisting of heavy metal/antiferromagnet bilayers [23], [24], operating by electric current pulses between 1 μs and 1 ms. These devices act as both binary and analog resistors making possible their integration in memory and neuromorphic applications. Examples of these material systems are Pt/PtMn, Ta/PtMn and Pt/$IrMn_3$ micropillars.

Additionally, UJI is actively working on all AFM tunnel junctions (MTJ) fully compatible with CMOS technology [25]. The materials of interest are antiferromagnets like $PtMn_3$ with induced texturization that promotes the spin splitting of the bands without the appearance of Spin-orbit Coupling. MTJs with 100% of tunnel resistance pave the path to the implementation of CMOS-compatible devices with multilevel bits compatible with 2 nm nodes.

UJI also conducts research for modeling fundamental physical mechanisms in advanced materials artificial intelligence. They combine experimental investigation and theoretical and numerical tools. *Halide perovskite* materials, which have been at the front of investigations of high-performance photovoltaic and optoelectronic devices, are known to contain mixed ionic-electronic conduction with significant hysteresis and memory effects [26]. Therefore, numerous authors are exploring halide perovskite devices, and the related class of organic materials, for building devices suitable for neuromorphic computing, including memristive devices and artificial neurons and synapses. UJI specializes in the analysis of devices by frequency domain methods (impedance spectroscopy), and the prediction and characterization of time domain response, such as potentiation transients in synapses [27], [28] and spiking of neurons [29]. UJI has explored material properties and performance of perovskite memristors, obtaining insight into the mechanisms of resistive switching [30]. They have also studied a range of materials technologies for brain-like computation, such as fluidic nanopores [31] and organic transistors [32]. A part of the group (Prof. J. Bisquert) is now in the process of transition to Universitat Politècnica de València (UPV), where they will continue their research.

Related to the use of magnetism for neuromorphic applications, Sort's group at Universitat Autònoma de Barcelona (UAB) has recently shown the potential of magneto-ionics, that is, control the magnetic properties of materials through voltage-driven ion motion. The utilization of electric field to gradually extract or reincorporate O^{2-} or N^{3-} ions in transition metal oxides and nitrides can be used to mimic synaptic functionalities, such as spike-timing and spike-amplitude dependent potentiation/depression effects or multi-state memory, all based on voltage-induced analog variation of magnetization [33]–[35]. The synergetic use of magnetic and electric stimuli to manipulate these materials (writing operations), and also to read them, offers added advantages compared to conventional memristors. Some challenges to be overcome are switching speeds at room temperature (sub-ms at the moment) as well as endurance, which so far is limited to thousands of cycles.

Graphenea Semiconductor is a *graphene foundry* headquartered in Donostia, Spain, and an office in Cambridge MA, US. It has over a decade of experience manufacturing graphene films and devices. Using standard semiconductor fabrication techniques, such as optical lithography, reactive ion etching (RIE), physical vapor deposition (PVD), or atomic layer deposition (ALD) among others, Graphenea fabricates a range of devices from 2-terminal resistors and 3-terminal field effect transistors (FETs), to 4-terminal Hall bars. Their process flows and techniques enable a myriad of devices to be implemented using graphene as an active layer, especially for sensory and photonic/optoelectronic applications. An extensive characterization capability, including Raman, AFM and electrical measurements, ensure that the devices manufactured are up to the specifications defined.

The versatility of Graphenea's process flows enables a myriad of device architectures to be implemented. For instance, a graphene memristor array for vector-matrix multiplication targeting AI applications has been implemented by researchers at Penn State University, and can be easily replicated/adapted to Graphenea's fabrication process [36]. In this work, a widely used cross-bar structure was implemented using the hysteretic properties of graphene FETs (GFETs) for multilevel conductance states. The device structure, a backgated FET through an ALD alumina layer as dielectric, does not rely on conductive filament formation as other memristor architectures, but on the trap states at the interface between the graphene and the backgate dielectric. The same group at the Pennsylvania State University also created a Physically Unclonable Functions (PUFs) using graphene FETs [37]. Using the normal distribution of carrier mobility and Dirac points and a simple analog to digital converter, the PUF implements a random number generator (RNGs) with nearly ideal entropy from the first bit. Besides its obvious application in numerous fields such as cryptography and security (or the Montecarlo method), this feature can be of value in hardware acceleration approaches related to (neuromorphic) AI.

The NeMeSys (Neuromorphic Memristive Systems) project is one of the most important and consolidated joint initiatives in Spain in the area of conventional and unconventional hardware cells for neuromorphic computing. NeMeSys brings together one CSIC research center and four national public universities: Institut de Microelectrònica de Barcelona (IMB), Universidad de Valladolid (UVa), Universidad de Granada (UGr), Universitat de les Illes Balears (UIB), and Universitat Autònoma de Barcelona (UAB). The consortium follows a multidisciplinary bottom-up approach that involves the fabrication, characterization, modeling, and simulation of memristive devices and systems. IMB focuses on the investigation of MIS and MIM devices with high-k dielectrics deposited by ALD such as HfO_2, Al_2O_3, and related nanolaminates [38]. The group specializes in the fabrication of both CBRAMs and OxRAMs and investigates the memristor ability to emulate synaptic functions [39]. UVa studies the influence of temperature and timing on the memristors dynamics [40], and the control of intermediate states for neuromorphic applications [41]. UGr builds tools for the simulation and design of memristors, and circuits including these devices [42], [43]. They also work on neuromorphic computing [44]. UIB focuses on device modeling [45] and circuit design with special interest in sensors, chaotic circuits, and cellular nonlinear networks [46]. UAB works in compact behavioral modeling of conventional [47] and unconventional memristive structures [48].

Finally, the Universitat Rovira i Virgili (URV) is developing physical oriented models and compact models of discrete flexible OTFT, organic devices, and simulate circuits for transforming electrophysiological signals into probabilistic bit streams using spiking neurons. The compact models consider the transient behavior and frequency, to find the range of operability, and test the limits of the technology. Some solution-processed/printable organic technologies such as inkjet printing, spin coating, and doctor blade coating, are being tested.

III. Circuits

Fig. 3 shows the main organizations involved in designing neuromorphic circuits in Spain.

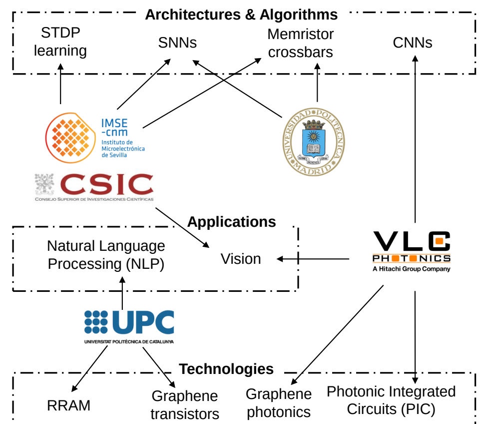

Fig. 3. Neuromorphic circuits Spain.

The Institute of Microelectronics of Seville (IMSE) has a long trajectory implementing SNNs in silicon for vision recognition applications. Based on hybrid *CMOS-memristor* technology, they have designed CMOL-like neuromorphic chips based on layers of CMOS integrate-and-fire neurons interconnected all-to-all through crossbars of 1T1R memristors, which represent the synaptic connections. The behavior of the memristors makes them especially suited to implement Spike-Timing-Dependent Plasticity (STDP) learning. In the proposed prototypes, the correlation between pre- and post-synaptic spikes is used to write or erase the corresponding 1T1R device, modifying the weight of the synapse it represents [49]. Although ideally these devices should be able to store analog information, they have been used as binary synapses (considering either high or low value) due to their non-ideal behavior [50].

The Universidad Politécnica de Madrid (UPM) has built neuromorphic circuits using memristors [51] with a focus on the design of interface circuits that can counteract non-idealities [52]. Currently, they are investigating how to implement spiking primitives with memristors (i.e. synapses and neurons) using FPGAs to accelerate and emulate SNNs [87], as discussed in Section V.

The Universitat Politècnica de Catalunya (UPC) is working on new computing paradigms using emerging devices, namely *Resistive Random Access Memory (RRAM) devices* and *graphene transistors*. They focus their RRAM research efforts on new digital structures for low-power in-memory computing [53] and neuromorphic systems centered on associative memories, as well as mechanisms to enhance neuronal functionality through stochastic resonance [54] and cellular automata for natural language processing [55]. Also, new structures and programming pulse (current and voltage) conditions of RRAM devices are being investigated focusing on their suitability for application as analog RRAM-based synaptic arrays and as part of neurons [56]. In the area of graphene technology, they have recently proposed binary and neuromorphic processing units using nanoribbon transistors and evaluating their sensitivity to structural defects [57].

Finally, VLC Photonics brings its expertise in Photonic Integrated Circuits (PICs) to drive advancements in neuromorphic photonic hardware, leveraging light's unique advantages like ultrawide bandwidth and low propagation loss [58]. Engaged in European projects such as POST-DIGITAL (see: postdigital.astonphotonics.uk), VLC Photonics contributes to the acceleration of the computation speed through PICs, from fundamental operations like matrix-vector multiplications [59] to optical signal recovery [60]. Branching into Convolutional Neural Networks (CNNs) via POST-DIGITAL, VLC Photonics aims to achieve terahertz-level operations to enable rapid and energy-efficient performance in tasks such as image recognition and object detection [61].

IV. Sensors

Fig. 4 shows the overall neuromorphic sensor and processor landscape in Spain, as well as end-user industry companies.

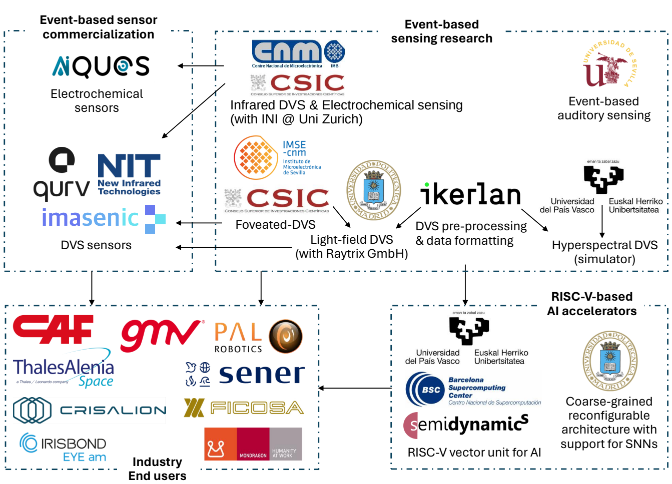

Fig. 4. Neuromorphic sensor and processor landscape in Spain.

Although one of the most important advantages of DVS sensors is the generation of information-efficient sparse data, the amount of produced events can still be large as the resolution of sensors increases especially when the DVS moves. To deal with this issue, IMSE has proposed the digital foveation mechanism inspired by the biological retina structure, reducing the pixel resolution dynamically in the background areas while keeping full high resolution in the Region of Interest (ROI). Implementing this mechanism in DVS sensors optimizes the generated visual information [62]. IMSE is currently collaborating with IKERLAN in the Horizon Europe NimbleAI research project (see: nimbleai.eu) to design and tape out a 300x400 pixel *Digitally-Foveated DVS (DF-DVS)* testchip using XFAB 180 nm process technology [63], [64].

In addition to the DF-DVS testchip, NimbleAI has built the world's first *Light-Field DVS (LF-DVS)* prototype that consists of a commercial Prophesee IMX636 DVS sensor coupled with a custom Raytrix micro-lens array, and demonstrated the feasibility of estimating depth using adapted light-field algorithms (originally designed for frame-based sensors) with time-surfaces created from LF-DVS inputs [64]. IKERLAN and IMSE, in collaboration with UPM-CITSEM and Raytrix, are now designing event-driven LF-DVS algorithms to enhance energy efficiency and achieve sub-ms latency. These algorithms are being prototyped on an FPGA before moving to ASIC implementation. LF-DVS has been highlighted in the 2024 Yole report on Neuromorphic Computing, Memory, and Sensing as an enabler for *neuromorphic 3D sensing* – expected to be ready by 2026 [65].

IMASENIC develops custom image sensor products. This includes neuromorphic solutions, where the emphasis is in the pixel design and data management. Namely, IMASENIC has designs of DVS pixels that can be coupled to standard image sensor pixels. The integration of the DVS pixels, with or without standard integrating pixels, is also boosted by 3D-stacking, which allows to integrate two CMOS layers: one optimized for sensing and the other for data processing [66]. IMASENIC technology is compatible with LF-DVS.

Besides visible, DVS technology has also been used in other ranges of the electromagnetic spectrum. Namely, recent developments by the IMB, in close collaboration with New Infrared Technologies (NIT), have demonstrated *Infrared DVS (IR-DVS)* compact pixel pitches to enable high-resolution, low-power, and high-speed IR vision [67], [68].

The University of the Basque Country (UPV/EHU), in collaboration with IKERLAN and CAF, are exploring a potential design of a *Hyperspectral DVS (HS-DVS)* to expand the applicability of snapshot hyperspectral sensors as part of the Basque SiliconBurmuin initiative [69] (bmh.gaia.es/neuromorphic). In the last years, the UPV/EHU has demonstrated the applicability of Imec's on-chip mosaic filtering technology [70] for image segmentation tasks in autonomous driving applications [71], overcoming the limitations of RGB sensors in terms of metamerism, and resulting in simpler and faster vision algorithms to discriminate objects based not only on their shapes but also on their composition. Building on [73], UPV/EHU has developed a customized event-based vision simulator that emulates the events that would be produced by a hypothetical HS-DVS using as input high frame-rate recordings with a snapshot hyperspectral camera featuring a VNIR 25-band hyperspectral mosaic sensor by Imec. A recording campaign has been carried out in CAF trains and the collected data are being processed and curated to produce an HS-DVS dataset, which will help select meaningful HS-DVS spectral bands and design associated event-driven algorithms.

Some of the DVS-based technologies above could be adopted by Qurv, which produces wide-spectrum image sensors based on CMOS-compatible colloidal quantum dot photodetector stacks [74]. In fact, the Qurv colloidal quantum dot-based process is CMOS technology agnostic and thus compatible with different types of analog in-pixel read-out circuitry. Hence a neuromorphic in-pixel circuit can be designed in CMOS technology to process the photocurrent injected from the colloidal quantum dot-based photodetector stack. Event-based colloidal quantum dot wide-spectrum image sensors would inherit all the benefits of visible image sensors such as low data rate, high speed, and high dynamic range while also allowing to sense infrared photons.

Beyond optical transduction, IMB is also designing neuromorphic microsystems based on solid-state sensors for the (bio)chemical analysis of aqueous solutions. The goal is to integrate neuro perceptive capabilities in situ, optimizing transduction, readout, computation, and communications in order to break the technical limits affecting the deployability, autonomy, versatility, and reliability of microanalytical systems in real-world conditions. In collaboration with the Institute of Neuroinformatics (INI) of the University of Zurich, IMB has achieved: (1) to establish novel neural processing methods to correct the sensor drifts and matrix effects so as to provide uninterrupted, multiple-week electrochemical monitoring from microsensor arrays in industrial settings [75]; (2) to demonstrate new prototypes incorporating silicon-based chemical sensors and machine learning methods for the continuous and non-invasive assessment of fitness from the markers observable in biofluids [76]; (3) to create the first implementation of electrochemical analysis using SNNs [77]; and (4) to introduce novel neuromorphic readout integrated circuits with built-in adaptive pulse modulation encoding for delivering sensor biasing, analog-to-digital conversion, and attenuation of unwanted background signals (such as DC offset and drifts) [78]. These innovations have prompted the creation of the startup AiQUOS to commercialize the technology.

The Robotics and Tech. of Computers Lab (RTC) of the University of Seville has developed a Neuromorphic Auditory Sensor (NAS) [79], [80] that mimics cochlea's Lyon model [81] in the spiking domain, getting rid of analog components or complex digital operations (i.e., multiplications or divisions). Using a small set of spike-based building blocks, it is possible to work in the Laplace domain to develop the required audition frequency decomposers. Converting audio signals to spikes, through low-power and low-computation generators [82], and feeding the resulting spiking signal to a set of concatenated spike-based band-pass filters, the NAS offers spiking activity for the different frequency channels of the input signal. Its cut-off frequencies, number of channels, and output interfaces can be configured dynamically.

V. Digital neuromorphic architectures

In NimbleAI, IKERLAN, BSC, UPV, and IMSE (in collaboration with Imec, CEA-List, Codasip, Raytrix, and 11 more EU partners) are designing a 3D silicon-integrated sensing-processing neuromorphic architecture that enables new modalities of event-based vision and 3D perception (i.e., DF-DVS and LF-DVS) with extremely low energy consumption and processing latency [63], [64].

In the *NimbleAI architecture*, a frugal always-on SNN-based sensing stage builds basic understanding of the surrounding visual scene to maximize the amount of meaningful visual information that can be captured and timely processed using computer vision solutions compatible with popular AI frameworks. More specifically, a DF-DVS layer in the top layers of the 3D stack work closely coupled with an SNN-powered early perception engine based on Imec SENeCA processor [83] that selects salient image features or ROIs. Visual event flows corresponding with selected ROIs are streamed to a Codasip RISC-V-based near-memory processing and inference tiles in the interior layers through 'visual pathways', which are dynamically created (and destroyed) as new ROIs are detected and foveated in the the DF-DVS. The visual pathways are independently configured based on the specific properties of each ROI (e.g., accuracy, latency), taking advantage of the irregular distribution of visual information and uneven temporal dynamics in the scene. Physically, they are implemented using Silicon Through Vias (TSV) across vertically-stacked layers. Logically, they rely on a 3D Network-on-Chip (3D-NoC) designed by the UPV. While developing the NimbleAI 3D-integrated architecture, system level trade-offs are being explored in a board-level prototype using 2D testchips (i.e., DF-DVS and SNN SENeCA) and a Xilinx MPSoC to implement digital processing designs, including event-driven LF-DVS stereopsis algorithms.

IKERLAN is designing BEGI, a SoC component to bridge neuromorphic and non-neuromorphic worlds and enable mainstream adoption of event-based sensors: IR-DVS, HS-DVS, LF-DVS, DF-DVS, and standard DVS. BEGI extracts meaningful information from DVS event streams and composes data structures (including depth maps when used with LF-DVS) compatible with AI models optimized to run on industry-standard processors and AI accelerators as well as on RISC-V CPUs, such as those by BSC [84], UPV/EHU [85] and Semidynamics. When combined with DF-DVS, BEGI provides best energy use by harnessing the sensor foveation mechanism.

The Center for Industrial Electronics (CEI) of the UPM has experience in implementing custom accelerator blocks for RISC-V-based SoCs. It has designed Coarse-Grain Reconfigurable Arrays (CGRAs) [86], accessible through custom ISA extensions, that offer functionality that can be adapted at run time through reconfiguration. The proposed CGRA is currently being extended to support neuromorphic operators in a general-purpose and configurable manner, including support from a custom MLIR-based compiler. This design will allow offloading compute-intensive operations in SNNs.

UPM has also developed Resnnance [87], a Python-based framework to automatically map high-level descriptions of SNNs to synthesizable RTL for implementation on FPGA devices. It works by mapping neuron layers to hardware cores for ultra-low area and power consumption, using deep pipelines for synaptic processing and distributed memory for weight and neuron states. At around 5.5 slices/neuron and only 348 mW, it is able to use 33% less area and four times less power per neuron than current state-of-the-art implementations. Using PyNN as a high-level interface, Resnnance is designed to support some of the most common layers in AI frameworks and ANN-to-SNN conversion flows.

VI. Neuromorphic computing and applications

Fig. 5 shows the organizations with activity in neuromorphic computing and applications in Spain.

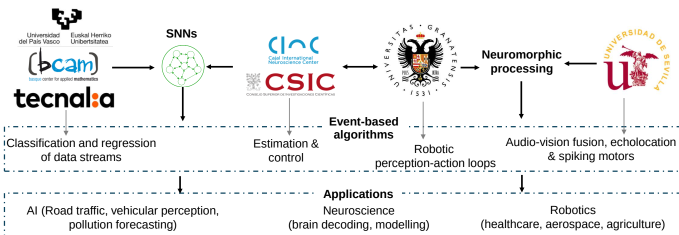

Fig. 5. Neuromorphic computing and applications landscape in Spain.

From the computational perspective, the Joint Research Lab on Applied Artificial Intelligence (JRL-A2I) led by TECNALIA, UPV/EHU, and BCAM have focused over the last decade on improving the performance and robustness of SNNs when used for different learning tasks, including classification and regression over data streams [88], concept drift detection and adaptation [89], outlier detection [90] and, more recently, the detection of novel inputs based on the characterization of spike trains throughout the neural architecture of these networks [91]. Such modeling achievements have exposed the enormous potential and competitiveness of this family of neuromorphic learners when compared to their non-spiking counterparts, showcasing their performance and energy efficiency in a diversity of applications including road traffic estimation [92], vehicular perception [93] and air pollution forecasting [94], among others. Currently this research activity within the JRL-A2I is shifting towards open-world continual machine learning, paradigm for which the sparsification of neural activations is essential to incorporate new knowledge to the network over time.

BCAM's Neural Automata (NA) is a relatively novel computational formalism within the class of Vector Symbolic Architectures, which maps symbolic computations (i.e. arbitrary partially computable functions or algorithms) to biologically plausible neuronal networks [95]. Using representation theory it maps computable functions and data to the neural network's activity space, all of which are transparently encoded in the synapse and activations functions. The NA framework paves the way for: (1) designing scalable neuromorphic circuits capable of advanced tasks (e.g. visual and language processing); (2) decoding the neural code and implementing neuromorphic circuits capable of communicating with biological neurons (see Section VI.A); and (3) designing efficient learning rules. As the NA can map a Universal Turing Machine to a neural network [96], the resulting universal neural network could learn or search for optimized biologically plausible neuronal networks for a given task. To date, BCAM has focused on mapping programs/data to Recurrent Neural Networks (RNNs) and they are now starting to explore mapping to SNNs. Likewise, BCAM has mathematically enlarged the classification of bursting patterns in SNNs and provided novel theoretical tools to construct complex spiking encodings [97].

The Neuro AI and Robotics (NAIR) group at the CSIC Centro Internacional de Neurociencia Cajal (CINC), in collaboration with the Donders Institute, is developing the theory and the algorithms for neuromorphic estimation and control for robotic [98] and neuroscience [99] applications. Namely, they develop SNN-based closed-form solutions [18], without the need of learning, for optimal estimation (Kalman-filter) and control (linear–quadratic–Gaussian). These neuroinspired networks provide sparse, irregular, and robust spiking patterns, similar to the ones observed in the brain. Hence, they have a huge potential for achieving low-power-low-latency robotic solutions. NAIR is further investigating learning to control dynamical systems with SNNs and the development of low-power-low-latency inference algorithms (see: spikeference.eu).

The CVRLab at UGr integrates asynchronous neuromorphic processing to close robotics perception-action loops in real-time. More specifically, they have demonstrated: (1) low-latency object tracking to anticipate trajectories in manipulation tasks [100], (2) early prediction of actions to forecast potential intentions of collaborators [101], (3) energy-efficient motion estimation to navigate dynamic environments [102],and (4) contour detection from sparse visual events for trajectory planning and obstacle avoidance – helping to identify boundaries and salient features in the scene [103]. These are all niche applications where efficient real-time neuromorphic vision has demonstrated superiority over classic computer vision methods [104].

The RTC Lab at the University of Seville has demonstrated the use of their NAS (see Section IV) for sensory fusion [105], [106] and echolocation for robotic navigation [107]. The RTC Lab has also used spikes produced by SNNs to drive motors, instead of classic PWM signals. A set of spike-based motor controllers are available, such as spiking-PID or bio-inspired ones, and have been integrated into robotic solutions. For example, the ED-Scorbot [108] is an industrial robotic arm based on a Xilinx Zynq device that integrates 6-SPIDs to control 6 DoF and allows the execution of Euclidean trajectories. This robotic platform allows the creation of datasets for training AI methods with hybrid information (i.e., spiking and non-spiking), which can be used for classification tasks, such as weight classification using SNN [109].

Finally, the GRVC Robotics Lab from the University of Seville has developed and experimentally validated event-based perception methods and schemes for autonomous navigation of flapping-wing robots [110]. They enable the online and onboard computation of event-based perception and control algorithms in tasks such as visual guidance [111] or avoidance of dynamic obstacles [112]. These applications fully exploit the main features of event-based vision including very low response times, high dynamic range, and robustness against motion blur, which is very relevant considering the vibration level produced during flapping [113].

A. Converging Biological and Neuromorphic Networks

In collaboration with UPM-CEI, the Center for Biomedical Technology (CTB) of the UPM is developing new microfluidic devices that build on their previous background in Organs-on-Chip to support cultures of neurons [114]. Thanks to the integration of electrodes, readout, and stimuli electronic circuitry, these neurons are currently being stimulated from an attached FPGA device, aiming to develop digital electronic twins of the biological networks and enabling a new type of computing fabric to carry out neuromorphic computation.

Likewise, BCAM is developing advanced closed-loop control algorithms that track, modulate or arbitrarily switch neuron activation patterns [115]. Combining dynamic-clamp technologies [116], advanced electrode interfaces and their NA approach [95], BCAM aims to design bioelectronic neuromorphic systems for machine-brain interfaces.

VII. Industry Alignment

Fig. 6 shows the main interest of Spanish end-user companies in the neuromorphic technologies discussed in previous sections. Note that materials, device, and circuit levels are not shown as they are not exposed directly to the end-users, but used to implement DVS sensors and SNN processors.

Sector	Company	DVS & DF-DVS	LF-DVS	IR-DVS	HS-DVS	NAS	SNN
Space	ThalesAlenia Space	◆		◆	◆		◆
	gmv	◆		◆	◆		◆
Robotics	PAL Robotics	◆	◆				◆
Autonomous vehicles	CAF	◆	◆		◆		◆
	CRISALION	◆		◆	◆		
	sener	◆	◆	◆	◆	◆	◆
	FICOSA	◆		◆	◆		◆
Machine-tool	Mondragon	◆	◆	◆	◆		◆
Medical & Healthcare	IRISBOND EYE am	◆		◆			◆

Fig. 6. Interest of end-user companies in neuromorphic technologies.

A. Space

The European Space Agency (ESA) and associated institutions have a significant interest in testing, validating, and advancing neuromorphic technologies to facilitate their widespread adoption in space environments and applications. These environments impose stringent requirements on reliability, including thermal resilience and radiation resistance, as well as reduced mass and power consumption. Neuromorphic technology is expected to help meet these constraints and enable build more robust and adaptable control systems for spacecraft, reducing reliance on ground control and thus allowing them to react to unexpected situations [117]. Interestingly, the inherent high dynamic range of DVS makes them appropriate to operate in space lighting conditions, which can change very quickly based on the relative position of spacecrafts with respect to a few high-intensity light sources. In ground exploration missions (such as Curiosity, Opportunity, etc.), power-efficient SNN-based vision systems are expected to enable real-time obstacle detection and path planning, allowing for autonomous operation.

GMV is using SNNs for hazard detection and navigation, including autonomous landing manoeuvres, as well as to efficiently process time-varying signals and handle noise and distortion more effectively compared to traditional DSP methods. Thales Alenia Space España is designing neuromorphic processing solutions for the telecommunication sector, specifically for interference detection and geolocalization [118]. Earth observation is another high-interest topic in which the company is working, porting CNNs to SNNs for more efficient on-board data processing and to alleviate downlink requirements. UPM collaborates with Indra in designing neuromorphic hardware for space and signal-processing applications [118].

B. Autonomous vehicles

Multimodal perception forms the foundation of Autonomous Driving Systems (ADS), which typically integrate RGB cameras, LiDAR, and radar sensors. However, ADS still face significant challenges, particularly when operating in adverse weather conditions and unpredictable and dynamic environments such as urban settings. Namely, low illumination, fog, rain, and glares, or highly reflective surfaces, can lead to missclasification of objects and missed hazard detections [119]. Although not commonly used, hyperspectral sensors have been proven to improve the robustness of ADS vision algorithms in adverse weather conditions [71].

Neuromorphic technology is expected to improve ADS systems by reducing the computational workload and response times to make safe driving decisions in real-time [72]. Furthermore, DVS brings inherent robustness against motion blur and lighting condition changes. As part of the Basque SiliconBurmuin initiative [69], UPV/EHU and IKERLAN are exploring the use of some of the neuromorphic sensor technologies discussed in section IV in CAF autonomous trains. Specifically, HS-DVS and LF-DVS are expected to provide energy-efficient, low-latency, and blur-free performance, along with robust spectral and 3D perception, enhancing object recognition even in low visibility conditions.

Ficosa, Sener, and Crisalion Mobility are also interested in testing neuromorphic sensors, processors, and algorithms in their ADS systems for autonomous cars and aircraft. IR-DVS is particularly appealing for use in autonomous cars, especially during nighttime driving, and NAS is expected to help identify the surroundings through sound identification.

C. Medical and Healthcare

Medical research has a growing interest in the DVS technology as it opens new perspectives in the diagnosis and treatment of neurological disorders. The high temporal resolution of DVS allows to quantify eye fixations and saccades as well as detect microsaccades (i.e., physiological oscillatory micro-movements). As part of the Basque SiliconBurmuin initiative [69], IIS Biobizkaia and Irisbond are exploring computerized tests that leverage the advantages of DVS to identify new eye biomarkers and accurately characterize existing ones. Their goal is to enhance early detection of degenerative diseases.

D. Robotics

The NAIR group at CSIC-CINC is at the proof-of-concept phase to evaluate SNN-based control of physical robots [18], including robotic arm manipulators, drones, exoskeletons and humanoids. The proposed SNNs are analytical to allow deployment to neuromorphic processors, and explainable to promote adoption opportunities by roboticists.

PAL Robotics is exploring the use of neuromorphic AI in the recently started Horizon Europe MANOLO and PRIMI projects (see: manolo-project.eu and primi-project.eu) to boost real-time sensory processing with a greater energy efficiency. This is expected to enable faster and safer robot responses and adaptations to dynamic and complex environments.

3D perception is of utmost importance in robot navigation, especially in robots that can move freely in 3D space like drones [120]. LF-DVS is expected to improve navigation of (lightweight) SNN-powered drones [17] by providing almost instantaneous (i.e., sub-ms latency) visual events enriched with depth, which could be used to efficiently estimate 3D scene flows [121]. Alternatively, DF-DVS facilitates the creation of multi-resolution maps of the surroundings as an initial step for estimating depth and optical flow, as demonstrated in [122]. This is particularly important to avoid obstacles when flying at high speed, execute precise maneuvers, implement SLAM, and support swarms of drones flying in close proximity in a coordinated manner.

Eye-tracking devices, like Irisbond's EYE am Hiru, facilitate human-robot interaction by detecting and transmitting eye-gazing information from humans to robots. Eye-trackers typically use near-infrared light to illuminate the eyes and capture reflections and hence, IR-DVS could help enhance the efficiency and wearability of these devices.

E. Machine-Tool

Industrial automation processes are at the core of most companies of the MONDRAGON Corporation. This involves using vision sensors and AI to enhance the performance of grinding, turning, milling, and boring operations, as well as to identify defects. DVS opens new opportunities for improving vision systems and production cells, including: (1) Count and measure size of objects moving at very high-speed in conveyors; (2) High-speed location estimation, guiding and fitting of objects for pick and place; (3) High-frequency vibration detection and characterization; (3) Continuous monitoring of liquid and plume flows; and (4) Tracking of small particles with spatter-like motion. IKERLAN, as the largest technology center of the MONDRAGON Corporation, is actively exploring uses of the neuromorphic sensor technologies discussed in section IV to create competitive advantages for the group companies. LF-DVS and HS-DVS are foreseen to be useful for discriminating particles and objects by composition and/or physical position as well as to better estimate the density of particle flows by gaining visibility at different flow layers. This is particularly interesting in additive manufacturing processes. Likewise, IR-DVS enhances efficiency when monitoring processes operating in the near-infrared spectrum, such as welding.

F. Biochemical

The biochemical analysis of aqueous media is a key activity to prevent environmental, health, and industrial risks, towards achieving the sustainable development goals in strategic sectors such as agri-food and water management. To tackle this challenge, AiQUOS is pioneering the application of neuromorphic microsensing and computing to monitor and control aquatic processes. By boosting energy and perceptual autonomy in a tiny mm-squared chip, neuromorphic analytical systems are poised to reduce acquisition and operation costs, enabling a full set of novel edge functionalities.

VIII. Conclusion

This paper provides an overview of the most important ongoing research activities related to neuromorphic technologies and applications in Spain. We believe these activities address well the objectives of the Spanish PERTE Chip program, which runs in liaison with the EU Chips Act. Currently, there are two main research projects that deal with neuromorphic technologies to mention: NeMeSys at the Spanish level (bringing together 5 Spanish partners) and NimbleAI at the EU level (involving 4 Spanish partners). The paper establishes connections between research on novel memristive materials and devices and the process flows of Graphenea Semiconductor, laying the foundation for creating a design and manufacturing chain for neuromorphic technologies in Spain. The paper also introduces the novel DVS technologies that are being investigated in Spanish organizations, which might well find their way toward commercialization through image sensor companies like NIT, Qurv, and IMASENIC, or by newly founded deep-tech startups.

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